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P3-7

Investigation of CVD-Co Silicidation for the Improvement of Contact Resistance

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1. Introduction

In present, $TiCl_4$-based CVD-Ti/TiN process is widely used to make a $TiSi_2$ ohmic layer in about sub-100nm contacts. But $TiCl_4$ based CVD-Ti/TiN process has some problems such as reactivity of $TiSi_2$ with dopant and rapidly increased contact resistance at small contact CDs. These problems of $TiSi_2$ have limited the implementation and extension of the CVD-Ti./TiN barrier metal process. A novel barrier metal process has been needed for achieving low BL/n+ and BL/p+ contact resistances in the next generation devices with sub-100nm. One of the solutions for these problems is the change of ohmic material from $TiSi_2$ to $CoSi_2$ which has inert characteristics with the dopants for contact ohmic layer.

Therefore, CVD-Co process can be a adequate alternative to CVD-Ti process in the development of next generation MOS devices[1]. Recently, Kang et al. have reported that the usefulness of CVD-Co process using CCTBA precursor which has a good step coverage, and which can be also extended to the silicide in 110nm contacts for achieving low contact resistances[2].

In this paper, the results of sub-100nm DC contact resistances with CVD-Co silicide are reported. we studied the reason of the degree of increase of Rc with decreasing contact size was lower with CVD-Co/Ti/TiN at small contacts compared to CVD-Ti/TiN. The mechanism responsible for Cobalt silicidation from CCTBA based CVD-Co in small DC was suggested by analysis of phase transformation and morphology of Co and Ti silicide.

2. Experimental

In this study, CVD-Cobalt fims were deposited in COMTECS MSCVD-8000™ system with CCTBA (Di**C**obalt Hexa**C**arbonyl **t**-**B**utyl**a**cetylene) and H_2. Process details and CVD-Co film properties were reported elsewhere[2]. In order to investigate the phase transformation of CVD-Co silicide in DC, samples for AES, XRD analysis were prepared on blanket Si(100) substrates. In the DC barrier metal process, Ti/TiN barriers were deposited by in-situ PE-CVD Ti and CVD-TiN after CVD-Co depositon, and W plug was deposited on TiN for acceptable small contact resistance. The bit-line spacer was constructed through LP-SiN process at 680°C for 7 hours, which was the thermal budget after the DC and bit-line formation.

DC resistances were measured at contact string with 10k contacts. SEM and AES were used to evaluate structural and qualitative analysis for the DC ohmic layers, respectively. XRD was also carried out to analyze Co/Ti-silicide formation after thermal budget.

3. Results and Discussion

Fig. 1 and 2 show the contact resistances with and without CVD-Co as a contact barrier metal. The contact resistance is drastically increased in the case of $TiCl_4$-based CVD-Ti/TiN at small contact CD. However, contact resistances remained at the level of 44% and 51% in BL/n+ and BL/p+ with CVD-Co in comparison to the CVD-Ti/TiN barrier metal at smallest contact CD. And when CVD-Co/TiN was adopted as a barrier metal structure in DC without CVD-Ti, BL/n+ and BL/p+ contact resistances were increased to about $10^7\Omega$/cnt. This result is different from the PVD-Co barrier. We suggested that impurities such as carbon or oxygen in as-deposited CVD-Co films piled-up at silicide surface and these impurities were removed by impurity gettering of Ti during the subsequent CVD-Ti deposition. So, CVD-Ti deposition is necessary after CVD-Co. Therefore, the investigation on contact silicidation of CVD-Co/Ti/TiN barrier metal structure was performed and presented as follows.

Fig. 3 showed the XRD analysis of CVD-Co/Ti and CVD-Co/Ti/TiN samples with and without thermal budget , since both of Co and Ti can form silicide on n+/p+ doped Si. For as-deposited CVD-Ti after CVD-Co, $CoSi_2$(111) and TiCoSi(013) on both n+/p+ doped Si was mainly observed, but $CoSi_2$(220) was mainly detected only on the p+ Si substrates. This difference of silicide phase with different doped substrates disappeared after thermal treatment at 680℃ for 7hours, and $CoSi_2$(111)(220), $TiSi_2$(022) peak was mainly observed on both n+/p+ doped Si.

AES analysis was shown in Fig. 4 and 5. Co depth profile after CVD-Co/Ti deposition at p+ Si sample was widely distributed inside film compared to n+ Si. But this difference of Co depth profiles at different doped substrates also disappeared after thermal treatment at 680℃ for 7hours, which is the same result with that from XRD spectra. Therefore, it is believed that Co silicide formed during CVD-Ti/TiN process may play a role in the barrier layer blocking the diffusion of Ti into Si diffusion. Therefore, it is suggested that the reason of lower contact resistance with CVD-Co was Co silicide could prevent unwanted $TiSi_2$ side reaction leading to increase of contact resistance during CVD-Ti process.

The SEM images of CVD-Co/Ti/TiN and CVD-Ti/TiN films are shown in Fig. 6. In the case of CVD-Co/Ti/TiN, uniform silicide layer was shown at both n+/p+ doped-Si. On the contrary, in the case of CVD-Ti/TiN, silicide morphology was very rough and uniformity was poor. These results suggest that Co silicide may act as a barrier layer resulting in reduced Si recess and improved silicide morphology. Especially, due to the formation of $CoSi_2$

interlayer, Si recess, which is not controllable, by the Si etching from $TiCl_4$, may be reduced and the morphology of silicide/Si interface may be improved. Decreased Si recess was better to obtain low contact resistance on both n+/p+ contact since Si recess could change dopant profile and Rp. And, because of to the inertness of Cobalt with the dopants and low solubility[3], Co silicide could decrease the dopant loss during CVD-Ti/TiN.

4. Conclusion

The improved of sub-100nm contact resistance with CVD-Co process was described. And the phase transformation and morphology of Co silicide is responsible for achieving the low contact resistance in DC.Co silicide can act a barrier layer and leading to decreased Si diffusion into Ti silicide during Ti silicidation. Co silicide may decrease the Si recess during $TiCl_4$-based CVD-Ti process. And due to the inertness of cobalt to the dopants, improved contact resistance was obtained.

CVD-Co contact silicide process is very promising solution for the next generation devices with sub-100nm DC contacts.

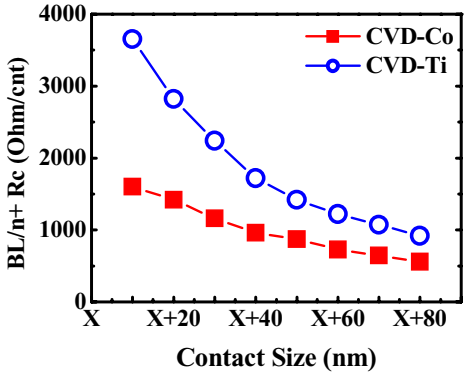

Fig. 1. Contact resistance of CVD-Co and CVD-Ti salicide on BL/n+ Si with various contact size.

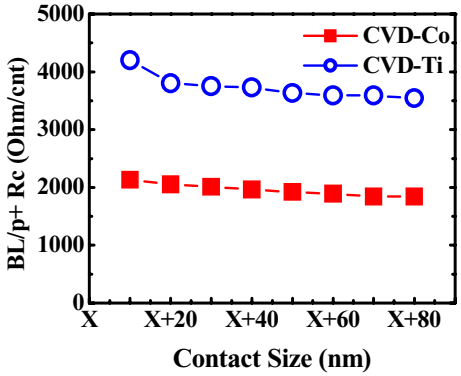

Fig. 2. Contact resistance of CVD-Co and CVD-Ti salicide on BL/p+ Si with various contact size.

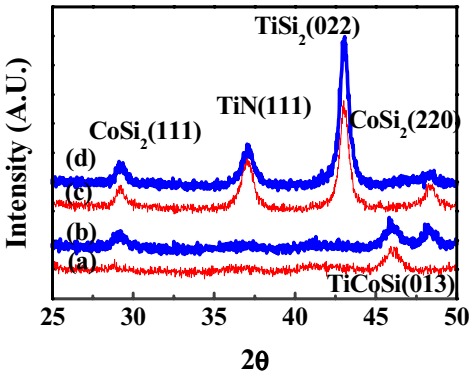

Fig. 3. XRD analysis of CVD-Ti/TiN after CVD-Co deposition for a) n+ Si/CVD-Co/CVD-Ti b) p+ Si/CVD-Co/CVD-Ti c) n+ Si/CVD-Co/CVD-Ti/ TiN with thermal budget and d) p+ Si/CVD-Co /CVD-Ti/TiN with thermal budget

5. References

[1] A.R. Londergan et al., *J. Electrochem.Soc.* P148, 2001
[2] S.B. Kang et al., *IEDM 2003*, P501, 2003
[3] V. Probst et al., *J. Appl. Phys.* v70, P693, 1991

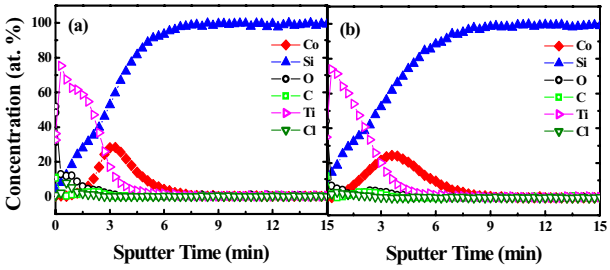

Fig. 4. AES analysis of CVD-Co/CVD-Ti silicide morphology on (a) n+ Si (b) p+ Si

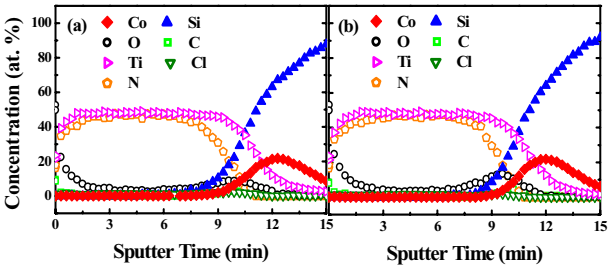

Fig. 5. AES analysis of CVD-Co/CVD-Ti/TiN/680℃, 7hr silicide morphology on (a) n+ Si (b) p+ Si

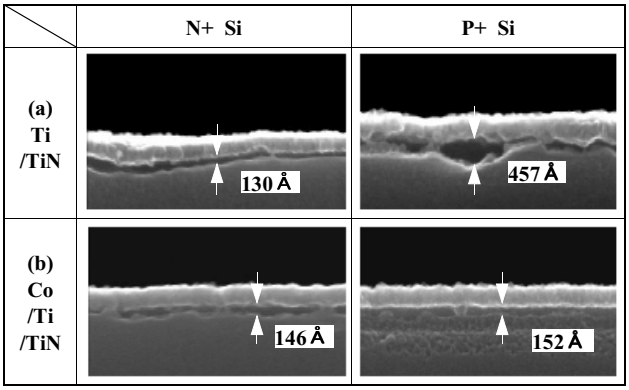

Fig. 6. SEM images of CVD-Co and CVD-Ti silicide morphology/(on n+/p+ Si)
(a) CVD-Ti/TiN (b) CVD-Co/CVD-Ti/TiN