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Modeling Geometry-Dependent Floating-Body Effect using Body-Source Built-In Potential Lowering for Scaled SOI CMOS

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1. Introduction

Sub-100-nm SOI CMOS shows the trend of coexistence of PD (partially depleted) and FD (fully depleted) devices, depending on channel length and width, in a single chip [1][2]. The floating-body effect, in other words, shows significant geometry dependence. This technological trend poses a challenge to SOI modeling [3] and its underlying mechanism merits investigation. Reference 1 has shown that the *body-source built-in potential lowering* (ΔV_{bi}) may represent the degree of full depletion (and thus floating-body effect) in SOI MOSFETs. In this paper we show that, similar to threshold voltage (V_T), ΔV_{bi} may exhibit reverse narrow-width effect, reverse short-channel effect as well as short-channel effect. Moreover, we demonstrate that ΔV_{bi} and V_T is correlated. The implication, under the unified BSIMSOI framework [3], is also discussed.

2. Body-Source Built-In Potential Lowering

While V_T is determined by the front surface potential (ϕ), the floating-body effect is determined by the SOI back surface. The coupled back surface potential at the source junction, ΔV_{bi}, can be probed by finding the onset of the external body bias after which the V_T and hence the channel current of the SOI device is modulated (Fig.1 inset) [1]. Fig.1 shows that the frontgate coupling induces ΔV_{bi} and in the strong inversion regime this frontgate-to-body coupling is shielded by the surface inversion layer, a manifestation of the correlation between ΔV_{bi} and ϕ.

This correlation, under the assumption of thick buried oxide, can be formulated by applying the Poisson equation in the vertical direction:

$$\Delta V_{bi} = \phi - Q_B / 2C_{Si} \qquad (1)$$

where $Q_B=qN_{ch}T_{Si}$ and $C_{Si}=\varepsilon_{Si}/T_{Si}$. Eq.(1) indicates that ΔV_{bi} increases when bulk charge Q_B (i.e., channel doping N_{ch} or SOI thickness T_{Si}) decreases, as verified by Fig.2.

3. Geometry Dependence of ΔV_{bi}

Short-Channel Effect

Fig.3 shows that ΔV_{bi} rolls up while V_T rolls off as L is scaled down due to charge sharing from the source and drain electrodes. The same basic double exponential functional form, derived from the quasi-2D short-channel effect for V_T [4], can be used to model the short-channel effect on ΔV_{bi}:

$$\Delta V_{bi} = \phi - Q_B / 2C_{Si} + \Delta V_{bi,SCE} \qquad (2)$$

$$\Delta V_{bi,SCE} = \beta_0[\exp(-\beta_1 L / 2l)+2\exp(-\beta_1 L/l)](V_{bi}-2\phi_B) \qquad (3)$$

Notice that the ratio of L to the characteristic length l determines the enhancement of ΔV_{bi} and the further suppression of floating-body effect of short-channel SOI devices [3].

Reverse Short-Channel Effect

As the short-channel effect and $\Delta V_{bi,SCE}$ are put down by raising L/l using the halo/pocket implant, the impact of laterally non-uniform channel doping on the length-dependent floating-body effect may be assessed by the approximated average channel doping:

$$\Delta V_{bi} \sim \phi - Q_B(L) / 2C_{Si} \qquad (4)$$

$$Q_B(L) = qT_{Si} [N_b(L-2L_h) + N_h(2L_h)]/L \qquad (5)$$

where N_b, N_h, L_h represent background doping, average halo doping and halo characteristic length, respectively (Fig.4 inset). Eq.(4) predicts the coexistence of both PD nominal devices (ΔV_{bi}=0V) and FD long-channel devices (ΔV_{bi}>0V) with continuous variations in between for scaled SOI CMOS, which is verified by measured ΔV_{bi} (Fig.4). Also notice that V_T rolls up while ΔV_{bi} rolls off as L is scaled down.

Reverse Narrow-Width Effect

In Fig.5, the enhanced ΔV_{bi} (and therefore suppressed floating-body effect) caused by the width scaling can be attributed to the gate-field encroachment from the STI edges. It may enable FD narrow-width devices on a PD-SOI platform [2]. Since Q_B is effectively reduced by the fringing field, V_T rolls off while ΔV_{bi} rolls up as W is scaled down. This also suggests that, similar to V_T, the same basic 1/W functional form can be used to model the reverse narrow-width effect on ΔV_{bi}.

4. Correlation between ΔV_{bi} and V_T

The geometry dependence of ΔV_{bi} resembles that of V_T because of the following relationship:

$$\Delta V_{bi} = \phi - (T_{Si} / 6T_{OX})(V_T - \Delta) \qquad (6)$$

where $V_T = \Delta + Q_B/C_{OX}$ and $\Delta = V_{fb} + 2\phi_B$ (Δ is close to 0). Eq.(6) predicts that at $V_{GS}=V_T$, $\Delta V_{bi}(\phi=2\phi_B)$ is linearly dependent on V_T with a slope equal to $-(T_{Si} / 6T_{OX})$, as verified in Fig.6.

In other words, knowledge of V_T can be used to estimate $\Delta V_{bi}(\phi=2\phi_B)$ for SOI devices with various feature size. Under the unified BSIMSOI framework [3], $\Delta V_{bi}(\phi=2\phi_B)$ is used as an index to determine the operation of BSIMSOI in a per-instance manner to gain both simulation accuracy and efficiency. Notice that the need for multiple V_T/T_{OX} transistors for low active/standby power requirement in a single chip may also result in the coexistence of both PD and FD devices in the same circuit by design, as indicated by Eq.(6).

5. Conclusions

The geometry-dependent floating-body effect can be explained by the correlation between ΔV_{bi} and V_T. This study points out the underlying mechanism responsible for the coexistence of PD and FD devices in a single SOI chip.

Acknowledgements

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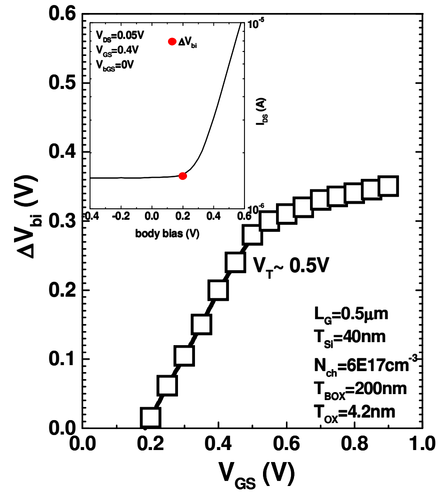

Fig. 1. Resemblance of ΔV_{bi} and ϕ as a function of V_{GS}.

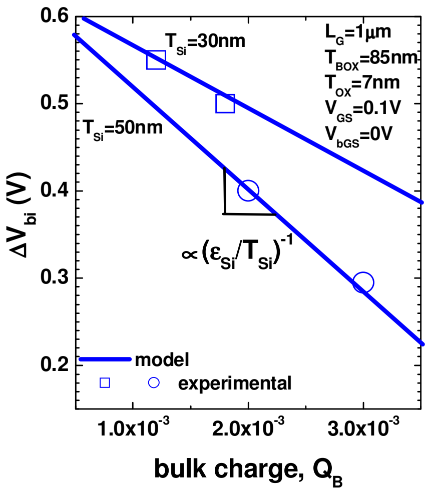

Fig. 2. ΔV_{bi} is an index of the degree of full depletion.

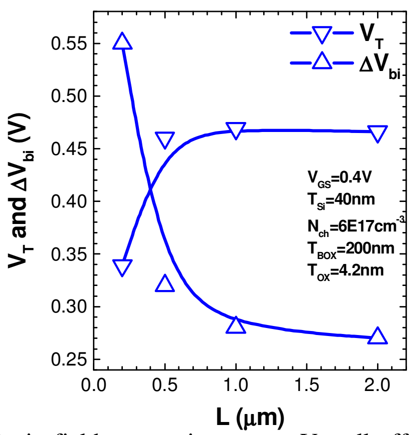

Fig. 3. Drain-field penetration causes V_T roll-off and raises ΔV_{bi} for short-channel SOI devices.

References

[1] P. Su et al., *IEEE EDL* **24** (2003) 90.

[2] F.-L. Yang et al., *VLSI Symposium* (2003) 137.

[3] P. Su et al., *IEEE CICC* (2003) 241.

[4] Z. Liu et al., *IEEE TED*, Jan. 1993.

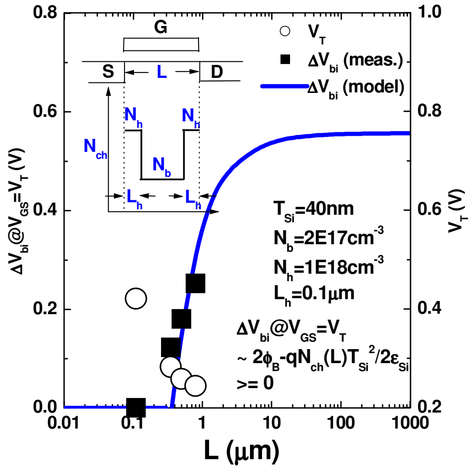

Fig. 4. The coexistence of PD/FD devices due to laterally non-uniform channel doping can be predicted by ΔV_{bi}.

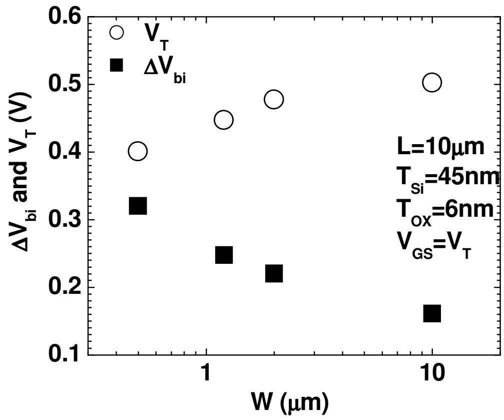

Fig. 5. Reverse narrow-width effect on ΔV_{bi}.

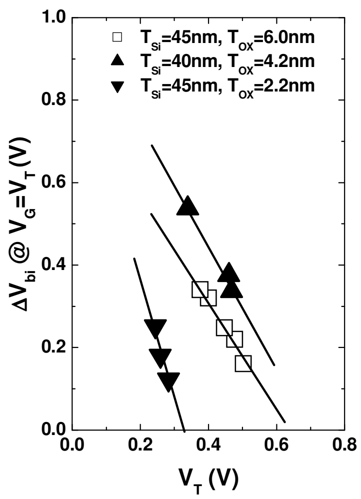

Fig. 6. Correlation between ΔV_{bi} and V_T.