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Width Effect on Hot-Carrier-induced Degradation for 90nm Partially Depleted SOI CMOSFET

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1. Introduction

Partially Depleted SOI MOSFETs (PD-SOI) was an attractive device due to the advantages such as full dielectric isolation and reduced junction capacitance which over bulk-Si device [1-2]. Especially for low-power digital and analog system, it is very attractive to apply narrow-width device fabricated on SOI substrate. However for SOI devices, there are very few studies on width effect of hot-carrier-induced degradation. It will be more serious as devices scaled down to 90nm with thin gate oxide (≦1.6nm). This work investigates the width effect on hot-carrier-induced degradation of 90nm PD-SOI device at various applied voltages.

2. Experiments

PD-SOI CMOSFET devices on IMplanted Oxygen (SIMOX) SOI substrates were fabricated with 190nm thick Si active layers, 150nm thick buried oxide (BOX), using the 90nm process with 1.6nm nitride gate oxide. Device HCE stressing and measurements were performed on probe stations using constant drain voltage (V_D=1.5V), and various gate voltage (V_G=0.75V~ 1.5V) with 400 minutes stress time

3. Results

Figure 1 shows the I_D-V_D characteristic of 90nm BC-SOI nMOSFETs with different gate widths, which was measured under constant gate voltage (V_G=1V). The I_D increases as the width decreases, which is presumably due to the increase of channel edge current [3]. In the subthreshold region, smaller width device possesses larger subthreshold drain current, causing worse subthreshold swing (Fig.2). For device with 1.2um gate width, the off state drain leakage (I_D @V_G=0V) is about 100 time than that of device with 10um gate width. Because of the contribution of the channel edge current, the transconductance (G_M/W) increases with the decrease of gate width and the threshold voltage of device has a negative shift, as shown in Fig.3. For smaller width device, we believed that the extra channel edge current will also cause higher gate leakage current (I_G/W) (Fig.4). The subthreshold swing and threshold voltage as a dependency of channel width was shown in Figure 5. For small gate width device, larger channel edge current in subthreshold region will cause the larger off state drain current, degrading device's subthreshold slope and decreasing threshold voltage. Figure 6 shows the I_D-V_D characteristic of 90nm BC-SOI nMOSFETs, which was stressed under constant drain and gate voltages (V_G= 1/2V_D=0.75V). In this work, only little drain current degradation was happened at short stress time (< 200 minutes). But after longer hot carrier stressing (>200 minutes), I_D was degraded rapidly. It is presumable that the thin gate oxide (1.6nm) was damaged severely after longer time stressing; thus the gate leakage current was increased (Fig. 7), resulting in device's I_D degradation. Same tendency was found in Figure 8 and 9 for device degradation. At shorter stress time, the I_D degradation was very trivial, but after longer stressing, the gate lost device's drain current control (Fig.8), causing very large drain current. For 90nm device, after longer hot carrier stressing, device possesses a positive threshold voltage shift and the device's G_M was decayed rapidly (Fig. 9). Figure 10 shows the lifetime versus various stressed gate voltages with constant stressed drain voltage (V_D=1.5V). 5% I_D degradation was chosen to identify the device's lifetime. It can be found that the lifetime decreased dramatically as the gate width decreased.

Figure 11 shows histogram distribution of I_{Dsat} for 90nm BC-SOI nMOSFETs with different gate width at various stress condition. Owing to channel edge current, no matter which stress voltage V_G=0.75 or V_G= 1.5V, the smaller width device possess larger stressing drain current density, thus inducing more interface defects. For width =1.2um, the device's I_D degradation with stressed V_G=1.5V (Fig. 12(a)) was always larger than that with stressed V_G=0.75V (Fig 12(b)); it is noted that larger degradation was not happen at V_G=V_D/2 (maximum I_{sub}), but at V_G=V_D [4]. It is presumably induced by the large vertical electrical field (T_{OX}=1.6nm) which increases inversion channel charge, causing larger hot carriers; therefore more serious valence-band electron tunneling was happened, increasing the interface state generation rate and I_{Dsat} degradation. For device stressed with V_G=V_D, small gate leakage variation (ΔI_G(%)) was found for device with W =10um and W=5um (Figure 13(a)). But for device with W=1.2um, I_G increased apparently over 10% after stressing 50 minutes, and then device's breakdown happened at 80 minutes. Same degradation tendency was found when device stressed at V_G=V_D/2 (Figure 13(b)), but the time to breakdown was enlarged, it is presumably due to lower vertical electrical field happen at lower V_G. We believed that at first the hot-carrier-induced defects happened at Si-SiO_2 interface, then larger generated defects is enough to cause the F-N tunneling, then the gate oxide breakdown happen with serious direct gate tunneling, resulting in large I_G degradation.

The hot-carrier-induced defects at Si-SiO_2 interface will causing device's threshold voltage shift, and provide a gate leakage path for carrier tunneling. Figure 14 shows the V_{th} shift versus hot carrier stress time. It is obvious that the V_{th} had a positive shift at first, and then the gate oxide breakdown occurred, resulting in device degradation. Same behavior was happened on $G_{M\,MAX}$ degradation. Figure 15 shows the $G_{M\,MAX}$ degradation versus hot carrier stress time. It is apparently that the smaller width device suffered from more serious $G_{M\,MAX}$ degradation. In this work, the device with W=1.2um shows serious device degradation and breakdown after 200min, while W=5um shows medium degradation especially after stressing after 350 minutes (Fig.15(b)); without breakdown happened on wider device (W≧ 5um) even at longer stress time. It is noticed that the degradation of device characteristic before device breakdown is very small. Thus for 90nm device with 1.6nm thin gate oxide, the gate oxide reliability will affect the hot-carrier-induced degradation especially for narrow gate width device. For narrow gate width device, the I_G degradation is very critical and always degraded suddenly at very short stress time (about 50 min in device with stressed V_G=V_D, 80 min in device with stressed V_G=V_D/2). Thus the gate width has have a great impact on the hot-carrier–induced degradation especially on deep submicron BC-SOI nMOSFETs with ultra thin gate oxide.

4. Summary

For 90nm BC-SOI nMOSFET with 1.6nm gate oxide, the width is a critical factor on the device reliability. Narrower gate width will cause device's V_{th} decreasing, edge current increasing, and hot–carrier-effect enhancing. For narrow gate width device, the I_G degradation is very critical and always degraded apparently. It is believed that the gate tunneling current is a major factor to affect the hot-carrier-induced degradation.

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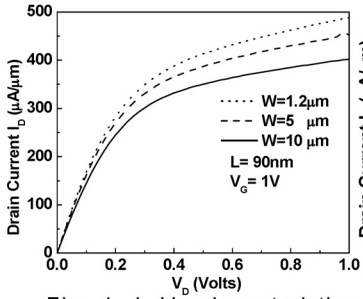


Fig. 1. I_D-V_D characteristics of 90nm BC-SOI nMOSFETs with different gate width.

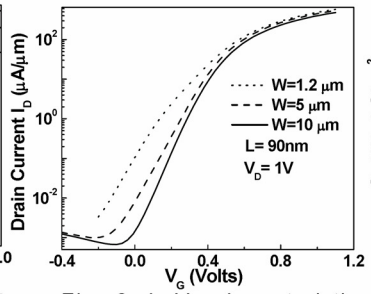


Fig. 2. I_D-V_G characteristics of 90nm BC-SOI nMOSFETs with different gate width.

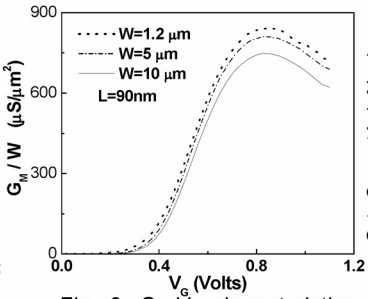


Fig. 3. G_M-V_G characteristics of 90nm BC-SOI nMOSFETs with different gate width.

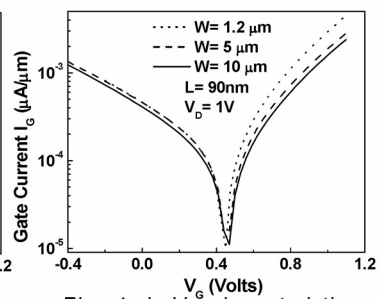


Fig. 4. I_G-V_G characteristics of 90nm BC-SOI nMOSFETs with different gate width.

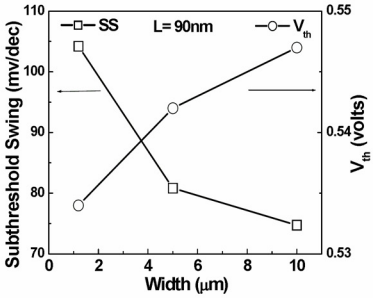


Fig. 5. V_{th} and Subthreshold swing of 90nm BC-SOI MOSFETs with different gate width.

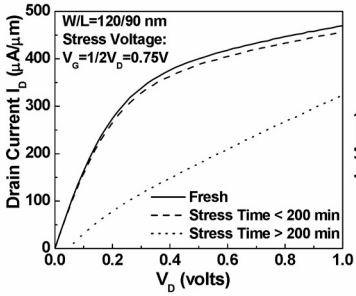


Fig. 6. I_D-V_D characteristics of 90nm BC-SOI nMOSFETs before and after hot carrier stressing.

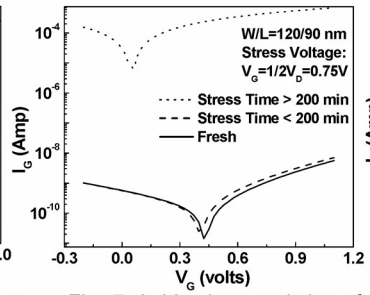


Fig. 7. I_G-V_G characteristics of 90nm BC-SOI nMOSFETs before and after hot carrier stressing.

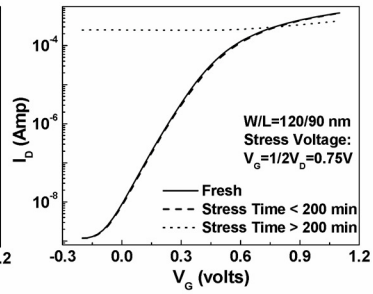


Fig. 8. I_D-V_G characteristics of 90nm BC-SOI nMOSFETs before and after hot carrier stressing.

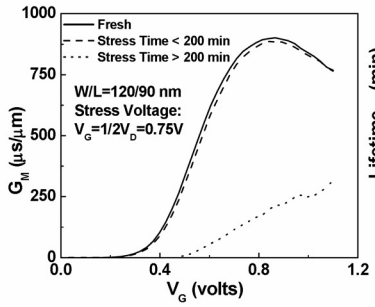


Fig. 9. G_M-V_G characteristics of 90nm BC-SOI nMOSFETs before and after hot carrier stressing.

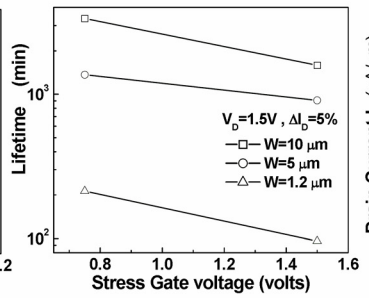


Fig. 10. Lifetime of 90nm BC-SOI nMOSFETs with different width at various stressed gate voltage.

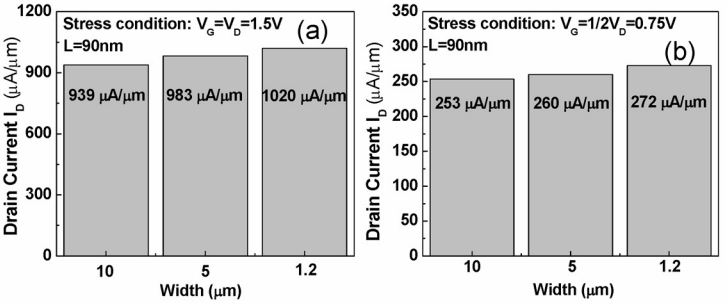
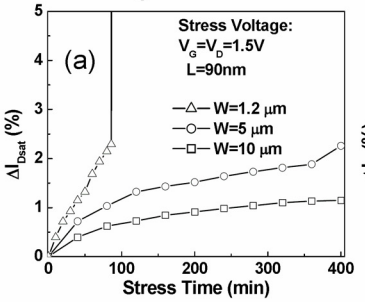
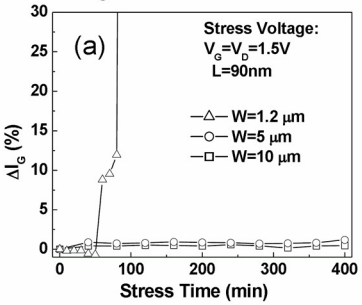
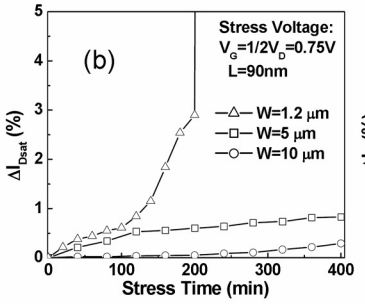


Fig.11. Histogram distribution of drain current for 90nm BC-SOI nMOSFETs with different gate width at various stress condition.







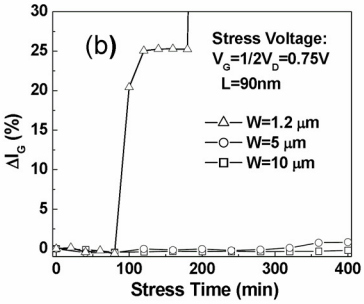
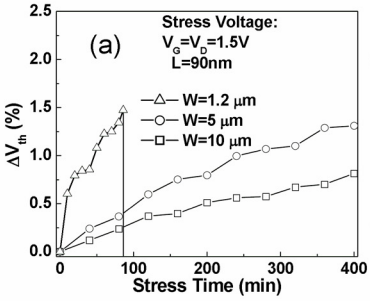
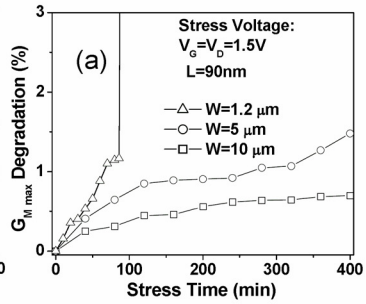
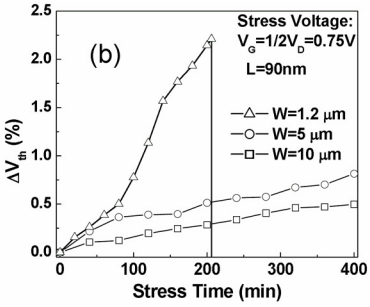


Fig. 12. I_{Dsat} degradation *vs.* stress time at (a) stressed V_G=1.5V (b) stressed V_G=0.75V for 90nm BC-SOI nMOSFETs with different gate width.

Fig. 13. ΔI_G shift *vs.* stress time at (a) stressed V_G=1.5V (b) stressed V_G=0.75V for 90nm BC-SOI nMOSFETs with different gate width.







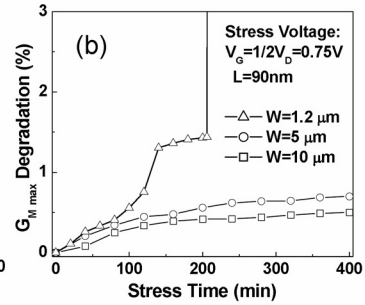


Fig. 14. ΔV_{th} shift *vs.* stress time at (a) stressed V_G=1.5V (b) stressed V_G=0.75V for 90nm BC-SOI nMOSFETs with different gate width.

Fig. 15. $G_{M\,mAX}$ degradation *vs.* stress time at (a) stressed V_G= 1.5V (b) stressed V_G=0.75V for 90nm BC-SOI nMOSFETs with different gate width.