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High-Performance Modified-Schottky-Barrier S/D p-Channel FinFETs

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1. Introduction

The 2003 ITRS roadmap predicts that metal gate and high-k dielectric will be used to improve device performance in the near future [1]. However, conventional source/drain (S/D) process requires a higher then 900°C thermal annealing for dopant activation and defect annihilation and such a high temperature process is not compatible with the metal gate/high-k dielectric. Schottky-barrier (SB) source/drain SOI MOSFETs have been proposed as possible nano device because of the easy process, low thermal budget, and small external resistance [2]. However, the drawbacks of small driving current, poor short channel effect and high leakage current make SB devices impractical [3-4].

In this work, we propose a novel modified- Schottky-barrier (MSB) device, which is featured with fully silicided S/D, ion-implantation to silicide (ITS), and low temperature diffusion processes. The I_{on}/I_{off} current ratio well exceeds 10^9. The S/D process temperature is only 600°C and is compatible with the metal gate/high-k dielectric process. Band diagrams at on-state and off-state are proposed to explain the device performance. At last, the hot-carrier reliability of the MSB devices is presented.

2. Device Fabrication

The key process steps and final structure of the MSB p-channel FinFETs are schematically drawn in Fig.1. The starting material was boron-doped ($1x10^{15}cm^{-3}$) SOI wafer with about 40 nm thick Si layer (Tsi). Device area was defined by e-beam lithography. The fin width (W_f) is about 60 nm. A 4 nm thick SiO_2 was thermally grown as gate insulator. Poly-Si gate was doped by BF_2^+ ion implantation. A pattern reduction technique was used to produce gate length (L_g) down to 49 nm. After gate patterning, SiO_2/Si_3N_4 composite spacer of 50 nm thick was formed. Nickel silicide was formed at S/D and gate region at 600 °C. The Si layer at S/D region was transformed to Ni-silicide entirely. The sheet resistance of the silicide layer is about 10Ω/□. Next, a BF_2^+ ions were implanted into silicide and were driven out at 600 °C to form a ultra-shallow S/D extension (SDE) at the silicide/Si interface and to modify the Schottky-barrier property[5]. Conventional non-silicided p-channel FinFET (CN p-FinFET) and simple Schottky-barrier p-channel FinFET (SB p-FinFET) were also fabricated. Fig.2 shows the in-line SEM top-view micrographs of the 49nm MSB p-FinFET.

3. Results and Discussion

The I-V characteristics of MSB, SB and CN p-FinFETs with L_g=49 nm, W_f=60 nm and T_{Si}=40 nm are compared in Fig.3, 4 and 5. It is clear that the MSB p-FinFET has much better driving current (~522 μA/μm @ $W=W_f$), I_{on}/I_{off} ratio (>10^9), swing (64.5mV/dec) and DIBL (39mV/V).

When the device is biased at on-state, the Schottky barrier of the MSB device is effectively thinned out so that the carrier can tunnel easily. Therefore, the excellent driving capability of the MSB device can be explained by the Schottky-barrier narrowing due to the ultra shallow SDE at the interface between silicide and channel. On the other hand, as the device is biased at off-state, the energy barrier at drain side of the MSB device is wider and higher than that of the simple SB device. The schematic band diagrams at on-state and off-state are shown in Fig.6 and 7, respectively. In practical, because of no implantation-induced defects, the I_{off} of the MSB p-FinFET is even lower than that of the CN p-FinFET. At high gate voltage, field enhanced band-to-band tunneling explains the increase of leakage current as shown in Fig.3.

Fig. 8 shows the transfer characteristics of the MSB p-FinFET measured at temperatures from 100 K to 500 K. The off-state leakage current decreases with the decrease of temperature and the I_{on}/I_{off} current ratio can well exceed 10^{10} at liquid nitrogen temperature.

The hot carrier reliability of the MSB p-FinFET is also investigated. Degradation in device performance under $V_g=V_d$ was tracked over time for the MSB p-FinFET with W_f=60 nm. As shown in Fig. 9, because hole trapping dominates the degradation, the magnitude of V_t increases with increasing stress time. Hot-carrier DC lifetime is also plotted in Fig. 10. The criteria of failure used for the plot is 10% change of gm (transconductance). These results indicate that the MSB p-FinFET with narrow W_f should be able to meet the 10 years lifetime requirement under normal operating condition.

4. Conclusions

A novel MSB p-FinFET with excellent electrical characteristics is demonstrated. The low temperature S/D process also relaxes the integration issue of metal gate/high-k dielectric. Simple process, excellent I-V performance, and competent hot-carrier immunity make the MSB FinFET a very promising nano device in the near future.

Acknowledgment

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References

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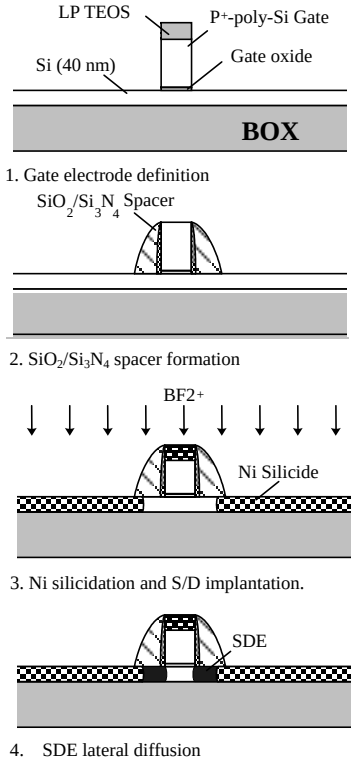

Fig.1 Key process flow of the MSB p-FinFETs.

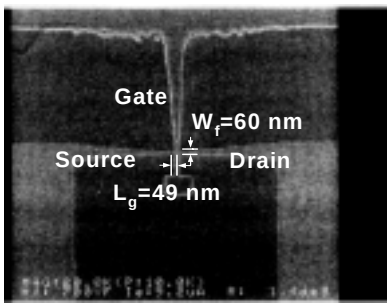

Fig.2 Plane view SEM micrograph of the fully silicided MSB p-FinFETs.

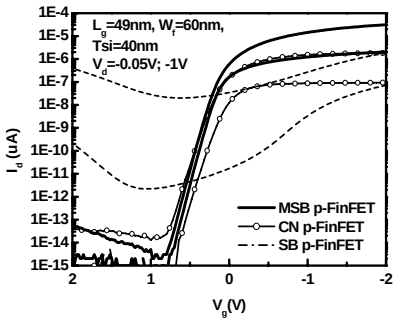

Fig. 3 I_d-V_g characteristics of the MSB, CN, and SB p-FinFET with L_g=49 nm.

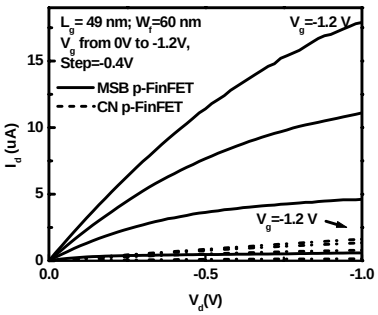

Fig.4 I_d-V_d characteristics of the MSB and CN p-FinFETs with L_g=49nm.

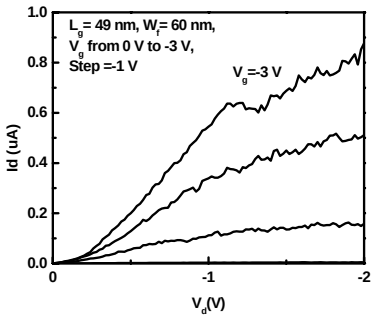

Fig.5 I_d-V_d characteristic of the SB p-FinFET with L_g=49nm.

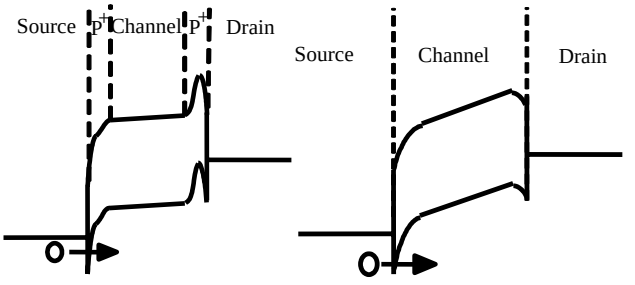

Fig.6 On-state band diagrams of (a) MSB p-FinFETs and (b) SB p-FinFETs.

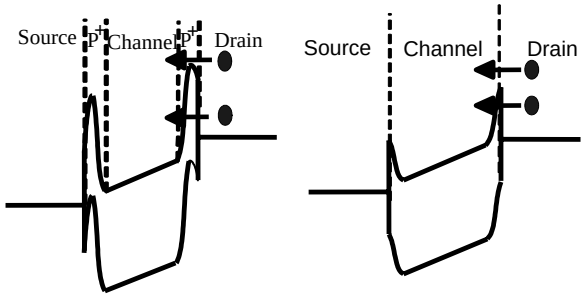

Fig.7 Off-state band diagrams of (a) MSB p-FinFETs and (b) SB p-FinFETs.

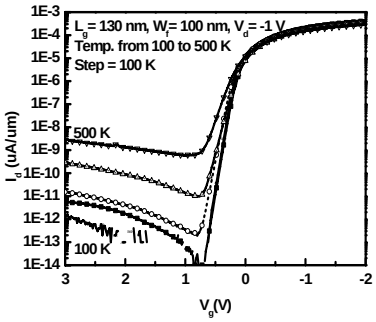

Fig.8 I_d-V_g characteristics of the MSB p-FinFFET at different temperatures.

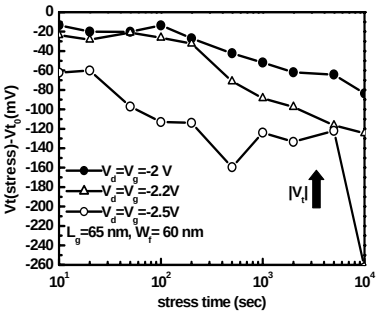

Fig.9 Threshold voltage shift of the MSB p-FiinFET versus stress time.

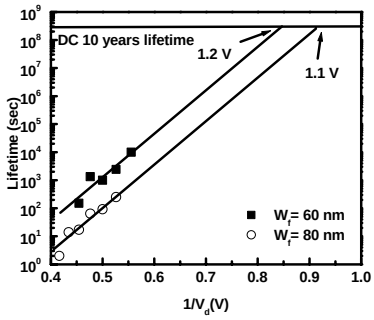

Fig.10 Hot-carrier lifetime projection of the MSB p-FinFETs with L_g=65 nm.