Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 498-499

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Nanoscale Strained Si/SiGe Heterojunction Tri-gate FETs

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1. Introduction

By incorporating the strained Si channels to enhance the carrier mobility and the strained Si/SiGe heterojunction to control the channel position, the strained Si/SiGe Tri-gate FETs have the enhanced current drive and the improved subthreshold swing in the NMOS, while the very limited enhancement of current drive and the degradation of subthreshold swing occur in the PMOS due to the buried channel conduction at the strained Si/SiGe heterojunction.

2. Device Structure and Simulation

The cross-section view of the proposed strained Si/SiGe Tri-gate FETs is given in Fig.1. The strained Si surrounds the embedded SiGe body, and the exact strain partition between the tensile strained Si and the compressively strained SiGe depends on the physical dimensions and thermal process of the device. For convenience, a fully strained Si and a fully relaxed SiGe are used in the simulation with the assumption that the strained-Si is thin enough or the strained Si/ relaxed SiGe is in the metastable state due to the low thermal budget. A channel doping of $10^{16}cm^{-3}$, dual polysilicon gate (n^+ for NMOS, p^+ for PMOS), 1.5 nm gate oxide, abrupt source/drain-to-channel junctions, and a $Si_{0.8}Ge_{0.2}$ body with fixed 5 nm surrounding Si are used in the 3-D simulation [1]. The mobility enhancement factors of 1.7 and 2 are used for electrons and holes in the strained Si respectively, while the SiGe body has a lower electron mobility of 0.25x and a lower hole mobility of 0.6x as compared to control Si. The type II band alignment of strained Si/SiGe heterojunction can have the electron confinement in the conduction band of the strained Si, and the hole confinement at strained Si/SiGe heterojunction. Fig. 2 shows type II band alignment of strained Si/SiGe heterojunction adopted in our study.

3. Results and Discussion

The control device has a higher electron concentration at fin center for the subthreshold and threshold bias, but has a surface conduction channel close to the Si/oxide interface at over threshold bias, while the strained Si/ SiGe device has a conduction channel in the strained Si at all three bias conditions (Fig. 3). The conduction channel closer to the Si/oxide interface for the strained Si/SiGe device at the subthreshold bias yields a better gate control, and thus a smaller subthreshold swing as compared to the control device (Fig. 4). The smaller fin width can make a channel closer to the Si/oxide interface and thus yields a smaller subthreshold swing for both devices. The subthreshold swings of both devices decrease with increasing channel length. The drain potential decay length L_D (Fig. 5) [2] increases as the fin width increases. The increase of drain-induced barrier lowering (DIBL) due to the increasing L_D yields a negative V_T shift at large fin width for both devices. Both devices have a V_T roll-off at short channel, but strained Si/SiGe device has a slightly smaller roll-off. The strained Si/SiGe device has a lower (more negative) threshold voltage (Fig. 6) than the control device due to the lower conduction band edge in the strained Si than that in SiGe (Fig. 2). DIBL characteristics of NMOS are summed in Table 1. Strained devices show better DIBL than controlled devices.

For the PMOS, the hole distributions of both devices have peaks at the fin center and form buried-channel conduction path in the subthreshold region. In the on-state, the strained Si/SiGe device has two conduction channels at the Si/oxide interface (surface channel) and the strained Si/SiGe interface (buried channel), while the control device has only a surface channel at Si/oxide interface (Fig. 7). The buried channel yields the inferior subthreshold swing of the strained Si/SiGe device as compared to the control device (Fig. 8). For both devices, the larger fin width has the conduction path away from Si/oxide interface in the subthreshold region, and yields larger subthreshold swing. Due to the band offset at the strained Si/SiGe heterojunction, the hole inversion layer can be formed at the less negative gate bias and the strained Si/SiGe device has a more positive V_T (Fig. 9). A worse threshold voltage roll-off of the strained Si/SiGe device is observed channel length and fin width decreases (Fig. 10). DIBL characteristics of PMOS are summed in Table 2. Strained devices are inferior to the controlled devices.

4. Summary

These novel strained Si/SiGe Tri-gate FETs with the enhanced carrier mobility and heterojunction confinement are demonstrated with greatly improved performance for NMOS by 3-D simulation. The PMOS is not improved as much as NMOS due to the buried channel at the Si/SiGe heterojunction.

References

[1] ISE TCAD Release 8.5, DESSIS 3D device simulator.
[2] G. Pei et al., IEEE Trans. Electron Device, **49** (2002) 1411.

Acknowledgements

This work is supported by the National Science Council, Taiwan, R.O.C., under the contract No of NSC 92-2215-E-033-004 (S. T. Chang)

Table 1 DIBL Characteristics of NMOS. Units of |ΔVt| and DIBL are V and mV/V, respectively.

NMOS	T=40nm		V_{DS}=0.05 V			
	Control			Strain		
L(nm)	45	65	80	45	65	80
Vt	-0.213	-0.174	-0.157	-0.257	-0.227	-0.215
	@ V_{DS}=1V					
Vt	-0.491	-0.292	-0.218	-0.475	-0.315	-0.259
|ΔVt|	0.278	0.118	0.061	0.218	0.088	0.044
DIBL	292	124	64	229	92	46

Table 2 DIBL Characteristics of PMOS. Units of |ΔVt| and DIBL are V and mV/V, respectively.

PMOS	T=40nm		V_{DS}=0.05 V			
	Control			Strain		
L	45	65	80	45	65	80
Vt	0.173	0.1399	0.1257	0.25547	0.2143	0.196
	@ V_{DS}=1 V					
Vt	0.445	0.26	0.184	0.542	0.34	0.265
|ΔVt|	0.272	0.12	0.058	0.286	0.126	0.069
DIBL	286	126	61	301	132	73

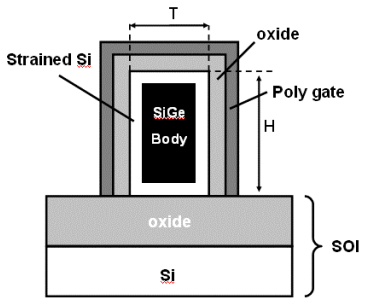

Fig. 1 Cross-section view of the strained Si/SiGe Tri-gate FET structure.

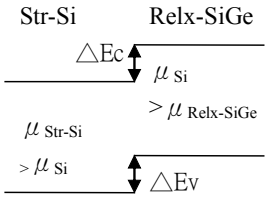

Fig. 2 Type II band alignment of strained Si/SiGe heterojunction.

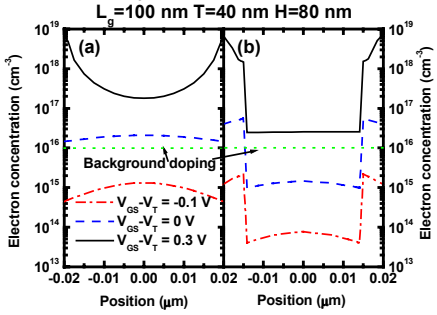

Fig. 3 Electron distribution along the lateral direction of Fig. 1 under three different bias conditions for (a) control and (b) strained Si/ SiGe NMOS. Bias conditions are (i) subthreshold region: V_{GS}-V_T = -0.1V (ii) at threshold: V_{GS}-V_T= 0V (iii) over threshold region: V_{GS}-V_T = 0.3V.

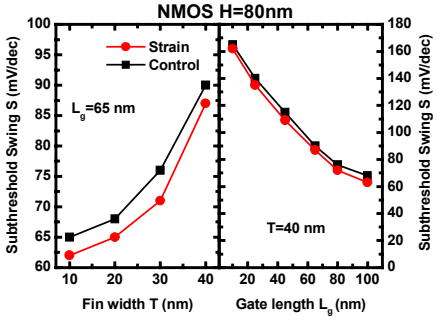

Fig. 4 Dependence of subthreshold swing on fin width T and gate length L_g. A narrower fin width shows lower subthreshold swing. The subthreshold swing is improved in the strained Si/SiGe device as compared to the control device.

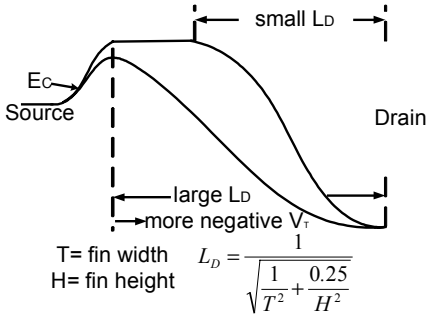

Fig. 5 L_D dependence on DIBL. Larger L_D has larger barrier lowering and yields a more negative V_T. H is the fin height.

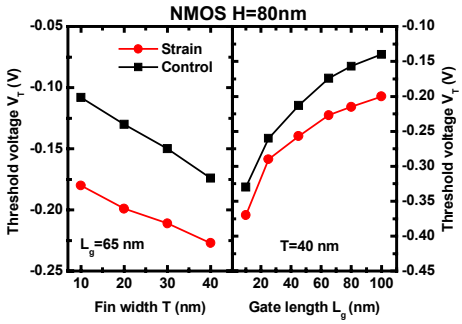

Fig. 6 Threshold voltage roll-off characteristics. Strained Si/SiGe device has a slightly smaller roll-off.

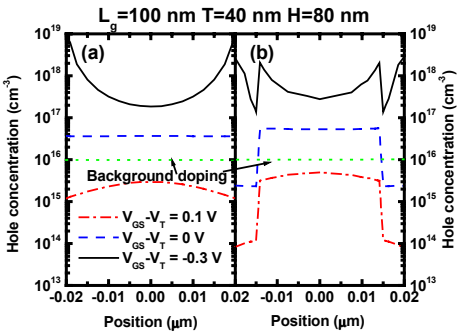

Fig. 7 Hole distribution along the lateral direction of Fig. 1 under three different bias conditions for (a) control and (b) strained Si/SiGe PMOS. Bias conditions are (a) subthreshold region :V_{GS}-V_T = 0.1V (b) at threshold region: V_{GS}-V_T = 0 V (c) over threshold region: V_{GS}-V_T = -0.3V.

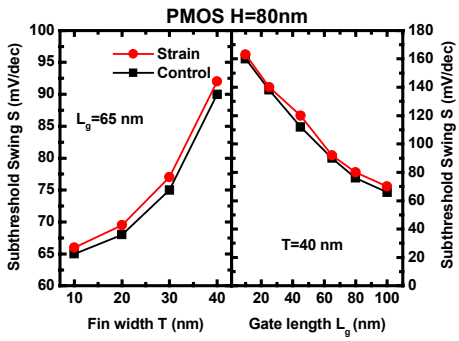

Fig. 8 Dependence of subthreshold swing on fin width T and gate length L_g. The strained Si/SiGe device shows higher subthreshold swing than the control device.

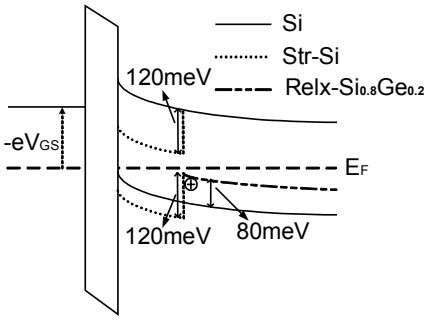

Fig. 9 The band diagram of the strained Si/SiGe device and control device. Due to band offset at Si/SiGe heterojunction, the hole inversion layer can be formed at less negative gate voltage.

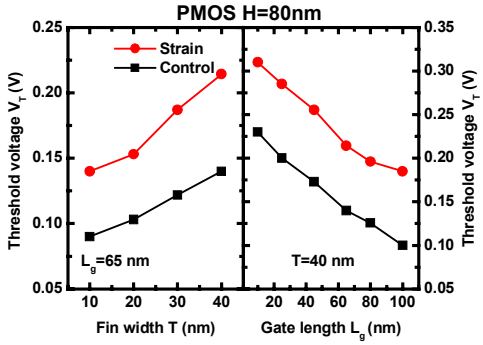

Fig. 10 Dependence of threshold voltage on fin width T and channel length L_g. The strained Si/SiGe device has a slightly larger roll-off.