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# Novel properties of erbium-silicided *n*-type Schottky barrier MOSFETs

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## 1. Introduction

As the gate length of metal-oxide-semiconductor field-effect transistors (MOSFETs) is reduced down to decananometer-scale, ultra-shallow junction formation techniques become great importance for the suppression of short channel effects [1]. However, one major drawback in the usage of ultra-shallow junction is the high parasitic series resistance. This obstacle can be overcome with Schottky barrier metal-oxide-semiconductor field-effect transistors (SB-MOSFETs) by replacing the impurity doped source and drain regions with silicides [2, 3]. The structure is quite simple and the ultra-shallow junction can be formed easily and accurately with very low parasitic source and drain resistance. Thus, SB-MOSFETs have been proposed as an alternative to the conventional MOSFETs for sub-100 nm applications [2, 3].

## 2. Experimental

In this work, erbium is chosen as source/drain metal of *n*-type SB-MOSFETs, because of its low Schottky barrier height (0.28eV) for electrons. Erbium silicide is formed by using rapid thermal annealing (RTA) technique. Annealing temperature and time is 500℃ and 5min, respectively. The formation of $ErSi_{1.7}$ phase is confirmed by x-ray diffraction (XRD) and Auger electron spectroscopy (AES) analysis. The sheet resistance of $ErSi_{1.7}$ is less than 30Ω/sq. even if the line width is less than 100nm. Thus, erbium is applicable in decananometer-scale SB-MOSFETs.

## 3. Results and Discussion

Fig. 2 shows drain current ($I_{DS}$) versus gate voltage ($V_{GS}$) characteristics of the 50nm *n*-type SB-MOSFET. The gate oxide thickness is 5nm. $I_{DSAT}$=120 $\mu A/\mu m$ with $V_{DS}$=1.0V, $V_{GS}$=3V and $I_{on}/I_{off}>10^5$ with low leakage current ($I_{LKG}$<10nA/$\mu m$). Experimental results are well described by newly developed theoretical model, giving the model parameters of SB-MOSFET, which is compatible with MOSFETs except one additional parameter, $\Phi_{bn}$ [3]. The increase of drain current with drain voltage can be explained by drain induced barrier thinning effect (DIBT) as depicted in Fig. 3, which is analogous to the drain induced barrier lowering (DIBL) effect in MOSFETs. However, the major mechanism of the increase of drain current in SB-MOSFETs is not the lowering of Schottky barrier height but the thinning of Schottky barrier thickness, giving the increase of tunneling current at low gate voltage, as shown in Fig. 2.

The abnormal increase of drain current ($I_{DS}$) with the decrease of gate voltage ($V_{GS}$) can be explained by hole carrier injection from the drain, which is confirmed by the theoretical analysis as shown in Fig. 4. In conventional *n*-type MOSFETs, the hole carrier injection from the source or drain is difficult because the junction can supply only one type of carrier, i.e., electron. But in SB-MOSFETs this is possible because the source and drain are composed with silicide. The metallic source and drain can supply both electron and hole, giving ambipolar characteristic.

One more novel characteristic of SB-MOSFETs is the increase of threshold voltage, compared with conventional MOSFETs. Fig. 5 shows the linear $I_{DS}$-$V_{GS}$ characteristic of SB-MOSFET. In Fig. 5, $V_{TC}$ represents the threshold voltage of conventional MOSFET, having the same process parameters except the source/drain structure, compared with SB-MOSFET. The extracted $V_{TC}$ value is 0.2V. On the other hand, the threshold voltage of SB-MOSFET is 1.34V as shown in Fig. 5. The increase of threshold voltage in SB-MOSFETs can be explained with the existence of Schottky barrier. Although the channel is inverted, there is no tunneling current until the tunneling barrier become sufficiently thin.

In Fig. 6, $I_{DS}$-$V_{GS}$ characteristics of 10nm ($L_{eff}$) *n*-type SB-MOSFET are simulated based on the extracted model parameters of 50nm SB-MOSFET. From the results, it seems that $I_{DSAT}$=600 $\mu A/\mu m$ is attainable using planar structure. One more important characteristic is that the subthreshold swing (SS) value can be less than 60mV/dec. This amazing characteristic is possible because there is no subthreshold drain current due to the existence of Schottky barrier.

## 4. Conclusions

In summary, erbium-silicided 50nm gate length *n*-type SB-MOSFET shows excellent transistor characteristics. The results show the possible usage of SB-MOSFETs in decananometer- scale as an alternative of conventional MOSFETs. This device shows novel characteristics such as DIBT, ambipolar carrier injection, increase of threshold voltage and very low subthreshold swing characteristics.

## References

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[3] M. Jang, Y. Kim, J. Shin, K. Park and S. Lee, Appl. Phys. Lett. 84 (2004) 741.

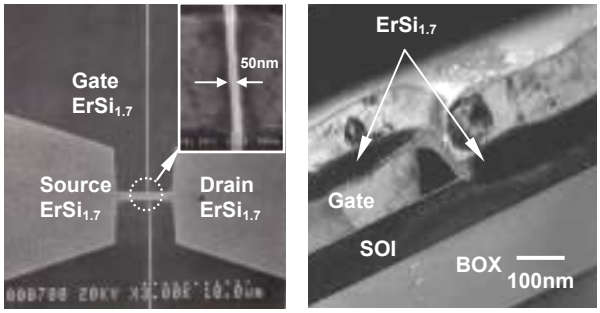


Fig. 1 SEM and TEM image of the erbium-silicided *n*-type SB-MOSFET.

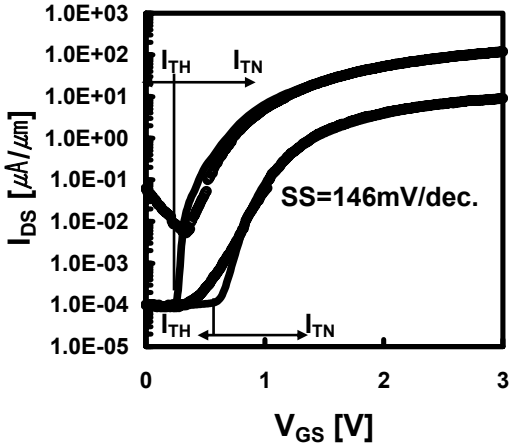


Fig. 2 Drain current ($I_{DS}$) versus gate voltage ($V_{GS}$) characteristics of 50nm *n*-type SB-MOSFETs with drain voltage of 0.1 (below) and 1.0V (upper).. The circle and solid line represents experimental and simulation results, respectively. In graph, $I_{TH}$ and $T_{TN}$ means thermionic and tunneling current dominant region, respectively.

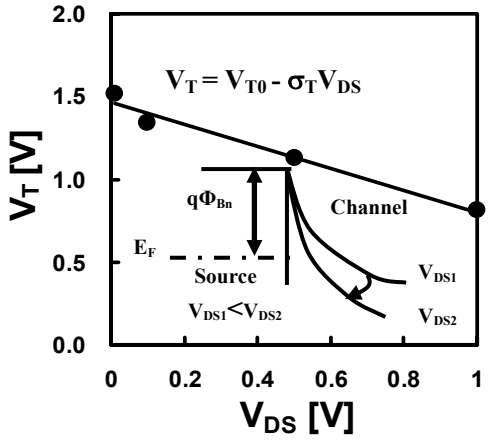


Fig. 3 Drain current ($I_{DS}$) versus gate voltage ($V_{GS}$) characteristics of 50nm *n*-type SB-MOSFET with the increase of $V_{DS}$ and the modeling of DIBT effect. The extracted threshold voltage ($V_{T0}$) and DIBT factor ($\sigma_T$) is 1.47V and 0.59, respectively

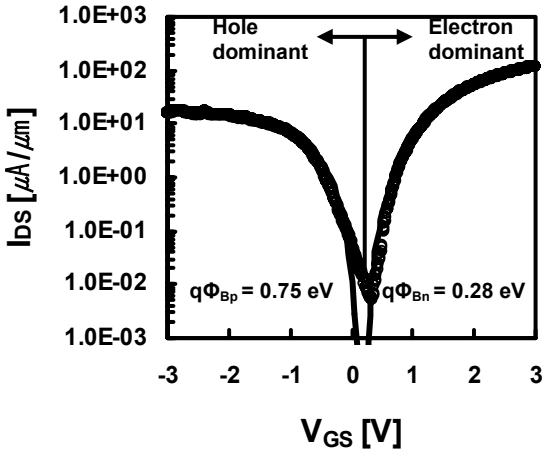


Fig. 4 Drain current ($I_{DS}$) versus gate voltage ($V_{GS}$) characteristics of 50nm *n*-type SB-MOSFET. Drain voltage is set to 1.0V. The drain current in negative and positive gate voltage region is caused by hole injection from drain and by electron injection from source. The solid lines represent theoretical calculation results.

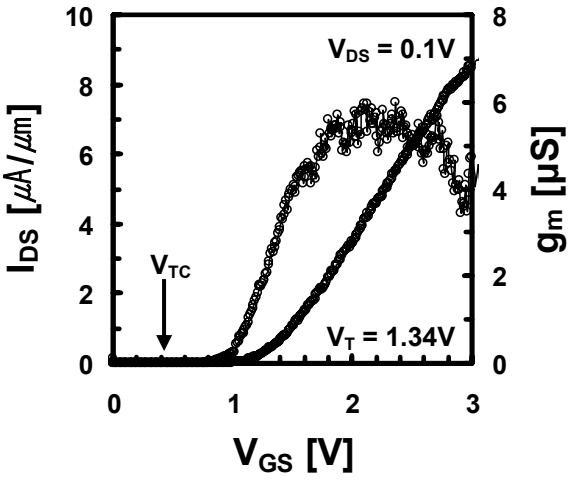


Fig. 5 The extraction of threshold voltage by $g_m$-max method in 50nm *n*-type SB-MOSFET.

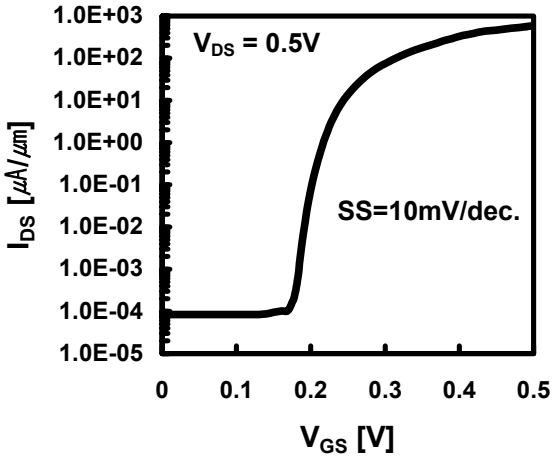


Fig. 6 Drain current ($I_{DS}$) versus gate voltage ($V_{GS}$) characteristics of 10nm *n*-type SB-MOSFETs (Simulation).