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A Selectable Logarithmic / Linear Response Active Pixel Sensor Cell with Reduced Fixed-Pattern-Noise Based on DTMOS Operation

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Abstract

A selectable logarithmic / linear response active pixel sensor cell with reduced fixed-pattern-noise is proposed. It is composed of four Dynamic Threshold MOSFETs, which have inherently less characteristics fluctuation than that of conventional bulk counterparts. Therefore it is expected that the proposed active pixel sensor cell should have reduced fixed-pattern-noise as compared with ones composed of bulk MOSFETs without any external noise reduction circuitry.

Introduction

CMOS active pixel sensors (APS) are now widely used for portable, low-voltage applications where power consumption is the major concern [1]. However one of the serious drawbacks of CMOS APS as compared with charge-coupled devices (CCD) is its fixed-pattern-noise (FPN) originating from the characteristics fluctuation, such as threshold voltage (δVth) and drain conductance (δId), of the devices comprising each pixel [1,2]. Thus one of the authors has already proposed a novel APS with reduced FPN utilizing DTMOS and demonstrated the possibility of FPN reduction [3] which is achieved by the fact that a DTMOS has inherently suppressed characteristics fluctuation as compared with that of a bulk counterpart [4].

In this paper the authors newly propose an APS cell also composed of DTMOS with selectable logarithmic / linear response. In addition to the three DTMOS used in its predecessor, the newly proposed APS cell has one more DTMOS that is responsible for logarithmic current-voltage conversion functionality. Since DTMOS has an ideal subthreshold slope in its weak inversion region theoretically independent of all device parameters such as gate oxide thickness, channel width and channel length, the resulting logarithmic current-voltage conversion functionality should also be ideal. In addition the authors propose a switching scheme to select either the linear- or the logarithmic response with operating bias conditions.

Basic Concepts

Figure 1 shows the equivalent circuit representation of the proposed photodiode-type APS cell with selectable logarithmic / linear response. Besides the functionality of M4, those of M1 through M3 are the same as those in the predecessor [3]. In linear response operation Vth of M1 determines the reset voltage of the photodiode; M2 is a source follower that converts photodiode voltage to signal current; and M3 functions as a data selector. δVth of M1 and δVth and/or δId of M2 are major origins of FPN of conventional bulk APS circuits [1,2]. Therefore replacing M1 and M2 with DTMOS should considerably reduce FPN. δVth and/or δId of M3 affects readout signal current, thus replacing M3 with DTMOS is also expected to reduce FPN [3].

In order to realize logarithmic response M4 is forced to be operated in weak inversion region through appropriately selecting bias voltages. This current-logarithmic voltage conversion is based on the fact that the drain current of a DTMOS in weak inversion region can be described as:

$$I_{ds}^{DT} \propto \exp\left\{\frac{q}{k_B T}\left(V_{gs} - V_{th}^{DT}\right)\right\} \qquad (1)$$

whereas that of a bulk MOSFET can be described as:

$$I_{ds}^{bulk} \propto \exp\left\{\frac{q}{mk_B T}\left(V_{gs} - V_{th}^{bulk}\right)\right\} \qquad (2)$$

(here q, k_B, and T stand for elementary charge, Boltzmann constant, and temperature, respectively, and m stands for a body effect coefficient which can be determined by $m = 1 + \frac{C_D}{C_{OX}}$ where C_D and C_{OX} stand for depletion layer capacitance and gate oxide capacitance, respectively.) Eq. (2) clearly indicates that the drain current of a bulk MOSFET in its weak inversion depends on the various device parameters. In addition V_{th}^{bulk} should change through the substrate bias voltage of M4, whose amount depends on the cathode voltage of the photodiode, which in turn is affected by the intensity of the incident light. This means that, because the argument (*i.e.*, $V_{gs} - V_{th}^{bulk}$) of the exponential function in eq. (2) also varies as I_{ds}^{bulk} changes in a bulk MOS diode, an ideal current-voltage conversion cannot be achieved. On the other hand, because the band bending is fixed in DTMOS due to gate-to-substrate connection, the gate depletion layer width in a DTMOS is also fixed and V_{th}^{DT} has a fixed value (where the surface potential is equal to $2\phi_B$ [4]; here $2\phi_B$ stands for twice of the potential difference between the Fermi level and the intrinsic Fermi level) independent from V_{gs}. Therefore $\left(V_{gs} - V_{th}^{DT}\right)$ is

independent from I_{ds}^{DT} and an ideal logarithmic conversion can be achieved through a DTMOS diode.

As summarized in Table 1 the response switching (logarithmic or linear) can be done through the bias voltage applied to RSTWL. When M1 is always in 'ON' state (i.e., RSTWL is always equal to Vdd), the proposed APS cell operates with logarithmic response. When M1 is used as the reset transistor in a conventional photodiode-type APS cell, it has linear response.

Experimental Results

Test circuits were fabricated using a conventional 0.6 μm 1poly 2Al processes with a 'bulk p-type Si substrate' through the VLSI Design and Education Center's chip fabrication service in Japan. Thus all of the DTMOS in the measured test circuits were pMOSFETs with respective individual n-wells, and, unfortunately, their Vth was not adequately adjusted for low voltage operation (Fig.2).

Figure 3 summarizes measured drain current characteristics of 12 pairs of respective two devices connected in series (corresponding amplifier M2 and source follower M3 in Fig.1). The ratio of standard deviation of Id to Id (σ_{Id}/Id) shown in Fig.3 clearly indicates the superiority of DTMOS in photodiode-type APS. σ_{Id}/Id in DTMOS pairs is much smaller than that in bulk counterparts as expected from the DTMOS operation principle [4].

Measured MOS diode characteristics comparison shown in Fig.4 also reveals that a DTMOS has not only superior logarithmic conversion characteristics to a bulk counterpart but also less characteristics fluctuation due to device parameters variation (*e.g.* channel length in this case). This means that the FPN originated from the variation in logarithmic conversion can be suppressed by using a DTMOS diode instead of a conventional bulk MOS diode. Therefore it is concluded that a DTMOS diode is an ideal device for photodiode-type APS cells with a logarithmic response.

Acknowledgement

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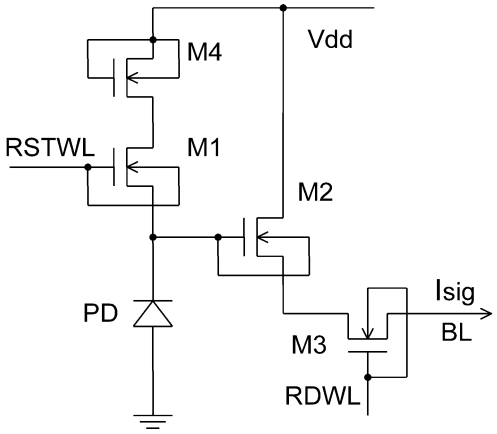

Fig.1 Circuit diagram of the proposed APS cell.

Table 1 Proposed voltage configuration.

	RSTWL	RDWL	BL
logarithmic response:	fixed at Vdd	0 V ↓ 0.6 V ↓ 0 V	high-Z ↓ low; readout ↓ high-Z
linear response:			
precharge	Vdd	Vdd	Vdd
photoconversion	0 V	0 V	0 V
readout	0 V	0.6 V	low

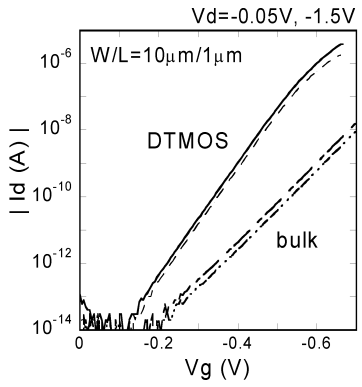

Fig.2 Measured device characteristics.

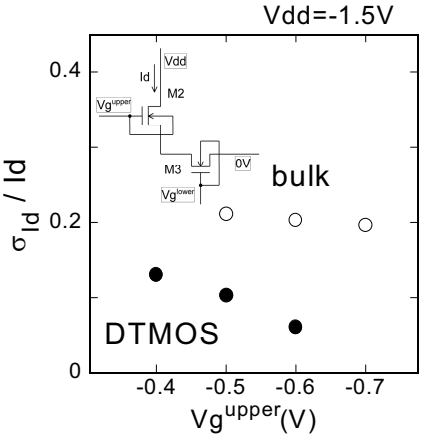

Fig.3 Measured σ_{Id} / Id for 12 respective device pairs.

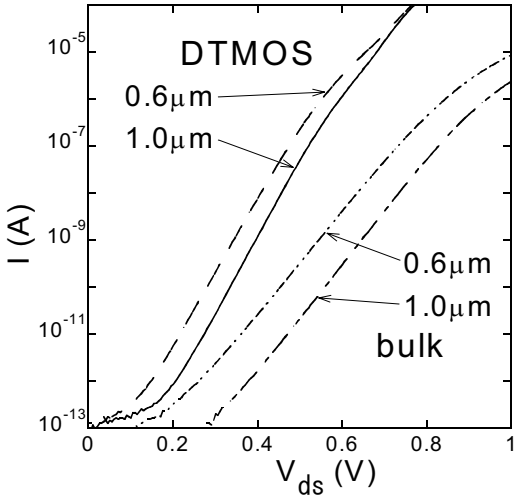

Fig.4 Comparison of measured MOS diode characteristics.