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Transient charging and relaxation in high-k gate dielectrics and its implications

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1. Introduction

DC characteristics of high-k gate dielectric such as mobility, Id-Vg, BTI and HCI have been investigated intensively, but the characteristics of high-k gate dielectrics at close-to-operation condition have not been studied in detail, assuming it will be similar to DC characteristics. However, recent studies showed that the transient charging in high-k gate dielectrics could have skewed most of DC stress based reliability characteristics [1,2]. In this paper, recent understanding on the effect of transient charging will be reviewed and its implications on test methods and high-k development will be discussed.

2. Definition of transient charging

Transient charging mentioned above refers to the charge trapping in high-k gate dielectrics accumulated during the device operation or the reliability stress. Transient charging can be classified into two categories depending on the characterization methods being affected. The first kind, fast traps, can affect the measurements with a characterization time in the order of μsec such as a single pulse Id-Vg, a DC Id-Vg with a short integration time and a mobility measurement. These traps are named as transient traps because most of traps can be detrapped easily when the device is turned off. The second kind, slow traps, can affect most of the reliability measurements such as TDDB, HCI, and BTI that are performed over the duration longer than seconds. These traps are also transient because most of the device degradations observed during these reliability tests are reversible.

3. Implications of fast transient charging

Drain current monitored while applying 100μsec and 1msec gate pulse shows a rapid current decrease due to the transient charging within the first tens of μsec (Fig.1). This pulse is repeatable because the transient charging decays off within a few tens of μsec. Fast transient charging distorts many DC measurements and changes significant portions of current understanding on high-k gate dielectrics. DC Id-Vg curve will be stretched as the measurement integration time increases because of the gate bias dependent concurrent charging (Fig.2). Swing and drain current of Id-Vg curve of TiN/Hf-silicate NMOS are improved with a shorter integration time due to the reduced charging. This result indicates that the conventional mobility measurement using DC Id-Vg underestimates the mobility of high-k dielectric. If the mobility of NMOS is calculated taking into account > 15% current gain shown at pulse Id-Vg curve, the actual mobility of TiN/Hf-silicate NMOS device will be significant higher than DC mobility and this mobility will be the characteristics of device in the real circuit devices operating at high frequency.

Understanding on transient charging effect provides various insights to the optimization of high-k gate dielectric stack. It is well known that the mobility of high-k gate dielectric can be recovered to the level of SiO_2 when the interfacial oxide layer is thicker than certain limit, typically 20Å [3]. This result can be simply understood as a result of reduced transient charging. Thus, the quality of interfacial layer will be a crucial factor in the improvement of high-k gate dielectric. Also, why hole mobility of high-k pMOS is not degraded as much as electron has been a long lasting question. Transient charging model explains that it is due to the lower transient hole charging. Another direction of mobility improvement is reducing the defects in high-k dielectric. However, little has been known about the nature of defects in high-k dielectrics or how to fix it. Recently, a high-pressure forming gas anneal is found to have a moderate effects [4], but this area needs significant study.

4. Implications of slow transient charging

Bias dependent device degradation of high-k devices during various kinds of traditional electrical stresses such as TDDB,

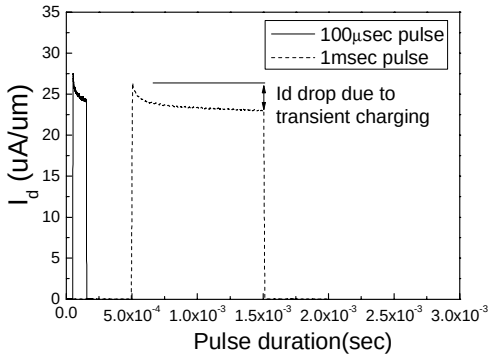


Fig. 1 Drain current measured using 100μsec and 1msec single pulse applied to gate. Pulse bias was 1.25V.

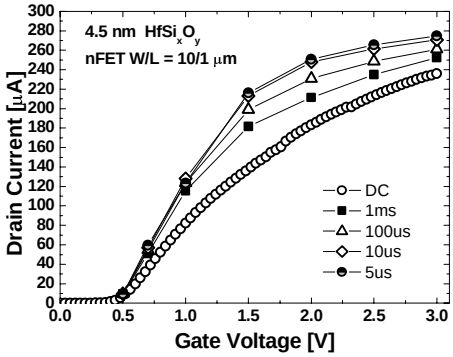


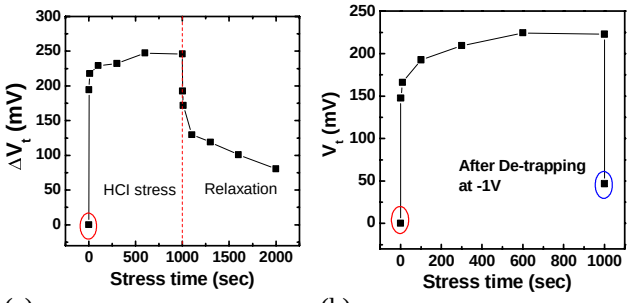
Fig. 2 Id-Vg curve measured with single pulse measurement. Each points of Id-Vg curves are drain current values measured and averaged during the pulse width in a range of 5μsec to 1msec.

NBTI and HCI can be attributed to slow traps. Previously, reliability characteristics of high-k films have been interpreted using the model developed for SiO_2 gate dielctrics. Unfortunately, several assumptions of oxide base reliability physics need to be revised because most device degradations observed at high-k devices are reversible, frequency dependent and may have different physical origins.

Device degradations during a hot carrier stress found to be dominated by the concurrent charging and those accumulated charges decay once the stress bias is turned off or can be completely detrapped using a proper negative bias (Fig.3, [1,2]). Thus, it is evident that previously reported hot carrier reliability of high-k device underestimated the lifetime by ignoring the contribution from concurrent charging. More importantly, hot carrier damage mechanism inherited from SiO_2 era should be reconsidered for high-k gate dielectrics even though the interfacial oxide layer may have some relevance.

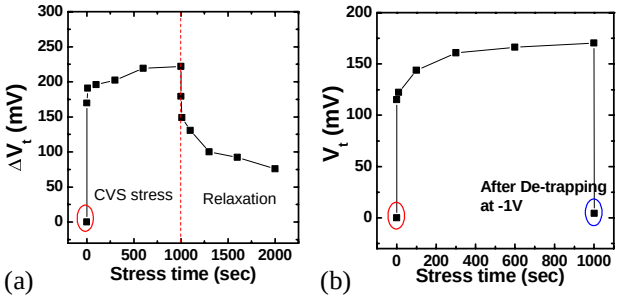
TDDB is another area that can be misinterpreted easily. Likewise HCI, V_{th} shift due to a constant bias stress is dominated by slow transient charging rather than bond breaking or trap generation and it is shown that the Vth can be recovered by detrapping (Fig.4, [5,6]). Thus, previously reported TDDB results are actually the results of accumulated charging and its impact on the electrical conduction in the film rather than the intrinsic reliability characteristics. Pulsed TDDB can partly avoid this problem and Y.H.Kim *et al.* reported the improved TDDB lifetime of high-k capacitors as the pulse width and duty cycle is reduced [6], but the intrinsic TDDB lifetime of high-k device needs to be extracted using much shorter pulse stress because the fast transient charging can affect the reliability evaluation also.

NBTI of high-k gate dielectric is more complicated than that of SiO_2. Under the negative bias stress, the interfacial layer of high-k gate dielectric is preferentially degraded and transient charging of NMOS is in detrapping direction (Fig.5,[7]). Thus, the effect of hole trapping and electron detrapping are mixed under the negative bias stress and the traditional meaning of NBTI such as Vth shift due to hydrogen bond breaking becomes a minor factor. Strong temperature dependent detrapping adds more complexity on NBTI evaluation. Thus, the usefulness of constant bias stress NBTI as a measure of device reliability is limited and more significant study on the polarity dependence and temperature dependence are necessary.



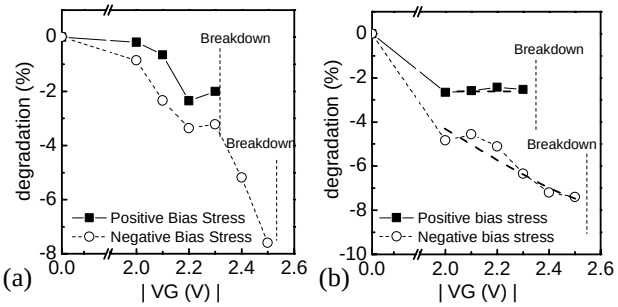
(a) (b)

Fig. 3 Hot carrier stress induced Vth shift and its recovery (a) during relaxation period or (b) using negative bias detrapping.



(a) (b)

Fig. 4 Vth shift during the constant bias stress and its recovery (a) during relaxation period or using negative bias detrapping.



(a) (b)

Fig. 5 Polarity dependence of stress induced device degradation; (a) gm and (b) Swing.

The above examples of HCI, TDDB and NBTI illustrated that the traditional bases of reliability study such as 1) extrapolation of high field stress reliability to low field stress reliability and 2) extrapolation of constant bias stress reliability to dynamic stress reliability are not necessarily valid for high-k devices. Although the elimination of transient charging itself might be a preferred way to avoid all of these complications, it may not be possible if it is related with the intrinsic properties of high-k dielectrics and more scientific approach to understand high-k dielectrics itself and to find the way to utilize those characteristics will be a realistic attitude towards the implementation of high-k dielectrics.

5. Conclusions

A novel transient charging model is proposed to explain the various characteristics of high-k devices such as mobility, HCI, and TDDB. Previously reported results on high-k gate dielectrics are interpreted using this model unifying the effect of slow traps and fast traps. The transient charging model suggests that most of the conventional electrical characterization methods used for SiO_2 gate dielectric need to be revised to account for the transient charging effect and the reliability physics of SiO_2 gate dielectric may not be directly extendible for high-k gate dielectric.

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