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Electrical Characterization of Strained Si/SiGe Wafers using Transient Capacitance Measurements

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1. Introduction

Strained Si (St-Si)/SiGe heterostructure shows great promise and rapidly approaches its practicality as an attractive candidate for fabricating high speed and low power CMOS. Many groups have studied its properties by structural and electrical analysis [1-6]. Among these evaluations, the electrical evaluation, especially the measurements for interface states (Nss) of gate oxide film/St-Si and minority carrier generation lifetime (τ_g) are very important because these two parameters are directly related to the device performance. In this work, Nss and τ_g were evaluated using deep level transient spectroscopy (DLTS) and MOS transient capacitance (C-t) methods. The dependences of Nss and τ_g on St-Si thickness (d_{Si}) and Ge fraction (Ge%) were shown clearly.

2. Experiment

The sample structure is shown in Fig. 1. The St-Si and SiGe layers were grown on 8 inch p-Si wafer by using CVD method. We prepared six kinds of St-Si/SiGe wafers and a bulk Si wafer, as listed in Table I, where N_A is the acceptor concentration. Since high temperature processing degrades the St-Si/SiGe heterostructure, we deposited SiO_2 films having thickness of d_{OX} on the wafers by using electron cyclotron resonance sputtering techniques at very low temperature of 130^0C. Then, the wafers were annealed at 450^0C in N_2 ambient for 30 minutes to improve the interface quality of SiO_2/St-Si [7]. After that, Al film having the thickness of 1 μm was deposited on the SiO_2 films by evaporation. The gate electrodes of 1mm diameter having the guard ring were fabricated by using lithography technique. The distance between the gate electrode and guard ring is 15 μm.

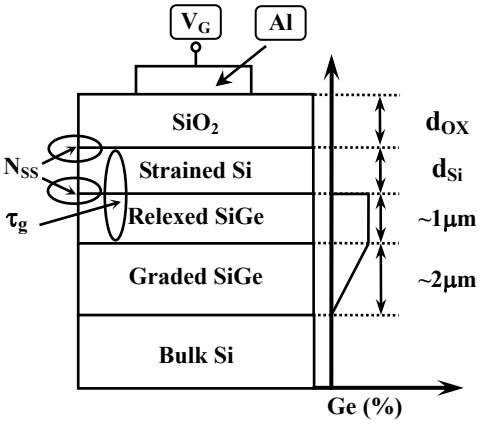

Fig. 1 Sample structure.

Table I Wafer parameters

Wafer	d_{Si} (nm)	Ge fraction (%)	N_A (cm^{-3})
A	100	25	6.4×10^{15}
B	25	25	1.5×10^{16}
C	20	25	1.9×10^{16}
D	20	30	2.2×10^{16}
E	20	20	1.5×10^{16}
F	20	10	1.2×10^{16}
G	Bulk Si	---	1.2×10^{15}

3. Result

Based on C-V measurement, we optimized the bias setting as V_G=+3V for DLTS measurement of Nss evaluation. The enough pulse height V_P=-8V was also confirmed by the saturated DLTS signal.

First, we measured Nss for wafers A, B, C and G to clarify Nss dependence on d_{Si}. Figure 2 shows the results, indicating i) the Nss of St-Si/SiO_2 and bulk Si/SiO_2 have similar values; ii) the Nss St-Si/SiO_2 has a fine value of about $1\times10^{11}cm^{-2}eV^{-1}$; iii) there is no clear dependence of Nss on d_{Si}.

Second, we measured Nss for wafers D, E and F in order to clarify the Nss dependence on Ge%. The results were shown in Fig. 3, indicating the increase of Nss with increasing Ge%. By using AFM measurements, we found the higher Ge%, the rougher St-Si surface. Thus we believe there is a strong relationship between Nss and surface roughness.

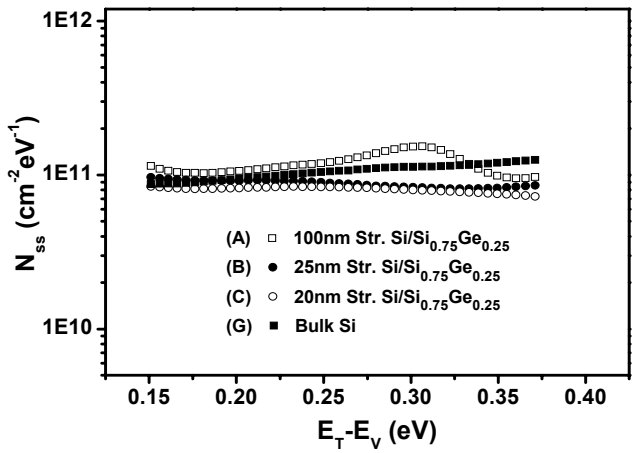

Fig. 2 Nss results for wafer A, B, C and G.

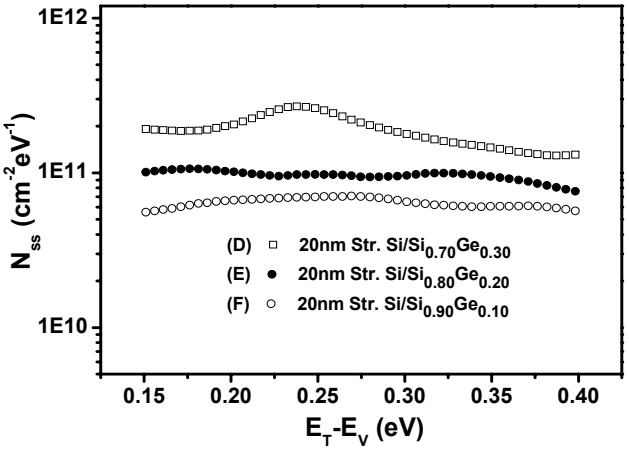

Fig. 3 Nss dependence on Ge fraction.

We also studied crystal quality dependences on d_{Si} and Ge% by measuring τ_g using C-t method. Based on C-V measurement and sample parameters, the step bias was set to V_{G1}/V_{G2}=0/+5V.

Fig. 4 shows C-t results for wafers A, B, C, and G. τ_g calculated by Zerbst-plot method were listed in Table II, which show clear dependence on d_{Si}. The reason is that

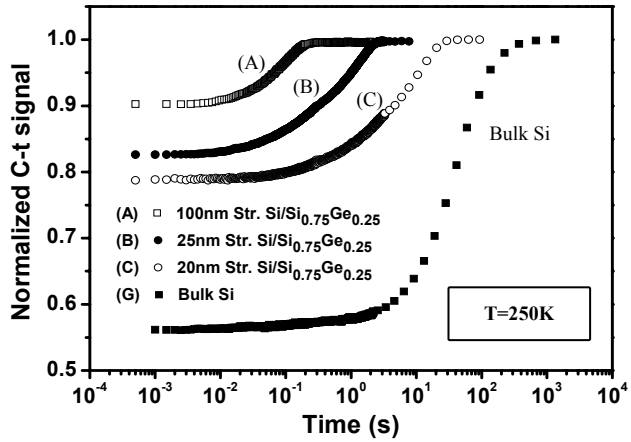

Fig. 4 C-t signals of wafers A, B, C and G.

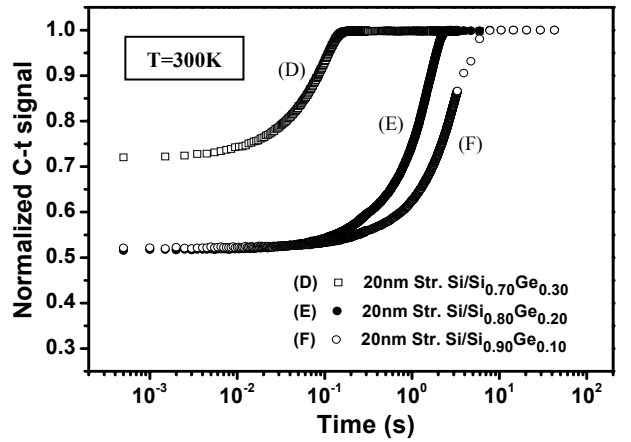

Fig. 5 C-t signals of wafers D, E and F.

Table II τ_g dependence on St-Si thickness and Ge fraction

Wafer	d_{Si} (nm)	Ge fraction (%)	τ_g (μs)
A	100	25	0.003
B	25	25	0.025
C	20	25	0.38
D	20	30	0.18
E	20	20	0.74
F	20	10	1.3
G	Bulk Si	---	1.0

thicker d_{Si} induces higher misfit dislocation (D_{mis}) density from interface of St-Si/SiGe to St-Si. In fact, TEM measurement enables us to observe the D_{mis} for 100 nm d_{Si} wafer.

Fig. 5 shows C-t results for wafers D, E and F. The calculated τ_g also strongly depends on Ge%, as listed in Table II. Even though the D_{mis} can not be observed by TEM measurement for 20 nm St-Si wafers, the defect source of τ_g reduction should be D_{mis} because D_{mis} density becomes higher with the increase of Ge%.

4. Conclusion

The Nss of St-Si/SiO_2 and τ_g of St-Si/SiGe were evaluated using DLTS and C-t methods for MOS structure. Nss shows independence on d_{Si} and obvious dependence on Ge%. The surface roughness of St-Si is the reason because of its enhancement induced by higher Ge%. τ_g shows strong dependence on both d_{Si} and Ge%. The defect source of τ_g reduction may associate with D_{mis} because D_{mis} density should depends on d_{Si} and Ge%. The Nss and τ_g for 20 nm St-$Si/Si_{0.80}Ge_{0.20}$ wafer are similar to those of bulk Si wafer. This means good wafer quality. Also Nss and τ_g for 20 nm St-$Si/Si_{0.80}Ge_{0.20}$ wafer by mapping measurement show good uniformity.

Acknowledgements

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