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Impact of Drain Induced Barrier Lowering on Read Scheme in Silicon Nanocrystal Memory with Two-Bit-per-Cell Operation

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1. Introduction

Silicon nanocrystal memory (SNM), where silicon nanocrystals (NCs) embedded in gate oxide act as storage nodes, is promising for high-density non-volatile memories [1-2]. One of the unique features of this memory is that SNM can store 2 bits per cell [3-5], that can be achieved by discreteness of the storage NCs and localized hot carrier injection. Electrons injected into NCs in the source side largely affect Vth, while electrons in drain side do not, resulting in distinguishable four states in the read operation. Fig. 1 shows schematically the four states: Erase, Write(D), Write(S), and Write(S+D).

There are two schemes to read the four states. Fig. 2(a) shows the typical read scheme (two-Vth scheme) where the device has two sets of Vth values [3,5]. Erase and Write(D) show very low Vth's and Write(S) and Write(S+D) has high Vth's in IV characteristics. In this case, two read operations are necessary by switching source and drain to distinguish the four states. On the other hand, we have shown that another read scheme is possible as shown in Fig. 2(b) where the device has distinct four Vth's (four-Vth scheme) [4]. Then, only one read operation is necessary to determine two bits. However, there has been no device design guideline for the suitable read operation of SNMs with two-bit-per-cell operation.

In this paper, device design of SNMs with the two-bit-per-cell operation is discussed in terms of the read schemes by analyzing experimental data and 2D device simulation. We will show the two read schemes are selected by controlling drain induced barrier lowering (DIBL). It is found that the four-Vth scheme is suitable for low voltage and low power applications.

2. Effect of drain induced barrier lowering

Fig. 3 shows measured IV characteristics of SNM [4]. Gate length Lg is 0.22 μm and Vds is 2 V. The simulation data, which is fitted to the measured data, are also shown. Four distinct Vth's are clearly observed, and this memory can be read by the four-Vth scheme. Fig. 4 shows the measured and simulated Vds dependence of Vth's in the four states. It is interesting to note that only Write(D) state has very strong Vds dependence, suggesting that DIBL is largely enhanced only in the Write(D) state.

In order to understand this phenomenon, the channel potential distribution is simulated. Fig. 5 shows potential distribution in the four states. When Vds is low (0.1V), the channel potential increases due to the injected electrons regardless of the injected position. This potential increase acts as a barrier and Vth increases. When Vds is high (2.0V), however, the potential barrier due to injected electrons in the drain side is lowered by the drain potential, resulting in large DIBL [3]. On the other hand, the potential barrier due to source side electrons remains even at high Vds. Therefore, Vth in the Write(D) state is determined by the amount of DIBL, and it can be controlled by changing device parameters that affect DIBL.

The Vth difference between Write(S) and Write(S+D) is also affected by DIBL, because the potential change due to drain side electrons in Write(S+D) is lowered by the drain potential, leading to similar channel potential and Vth to those of Write(S) at high Vds. The spatial distribution of injected electrons in source and drain side NCs also affects Vth's in the Write(S) and Write(S+D) states.

3. Design guideline of SNM

Here, we discuss the device design of SNM in terms of the read scheme. In order to utilize the four-Vth scheme, DIBL should be suppressed, that is, the short channel effect should be suppressed. The read voltage should be low, or gate length is long enough. Then, the reduction of Vth in Write(D) is minimized and the clear four Vth's are achieved. Therefore, the four-Vth scheme is suitable for low voltage and low power applications. On the other hand, the two-Vth scheme can be obtained in the memory with large DIBL. The read voltage should be high, or the gate length should be aggressively scaled. Fig. 6 shows simulation results for the device with shorter gate length (Lg = 0.15μm). Larger DIBL is clearly observed in Write(D) state at 2.0 V and Vth of Write(S) becomes closer to Write(S+D) at high Vds, resulting in the two-Vth scheme. Therefore, the two-Vth scheme requires aggressively scaled Lg with high read voltage.

4. Conclusions

Threshold voltages of SNMs with 2 bits per cell are examined by experiments and simulation. It is found that DIBL has a great impact on Vth's in the four states. Device design guidelines of SNMs are discussed in terms of the read scheme, and it is found that four-Vth scheme is suitable for low voltage low power applications.

Acknowledgements

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References

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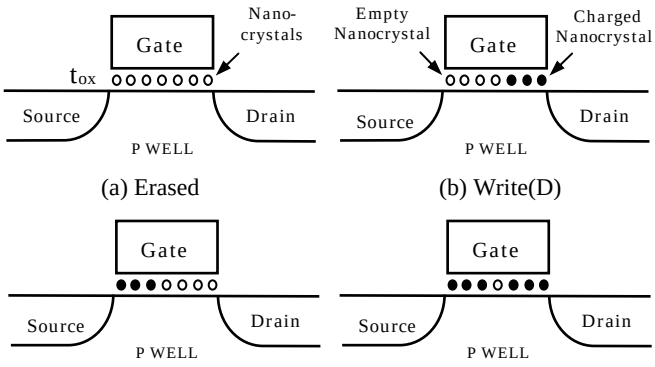

Fig 1. Schematics of the four states in SNM. (a) Erase, where all the NCs are empty. (b) Write(D), where NCs in the drain side is charged by the injected electrons while the NCs in source side is empty. (c) Write(S), where NCs in the source side is charged. (d) Write(S+D), where NCs in both sides are charged.

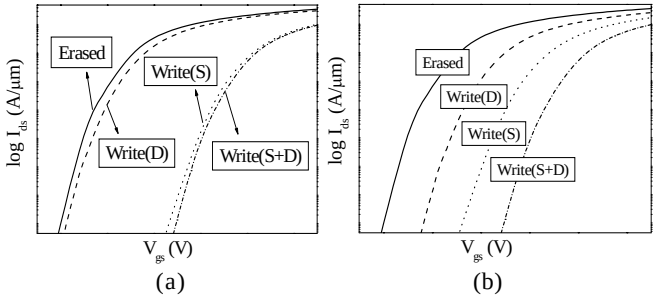

Fig 2. Schematics of IV characteristics of SNMs with two-bit-per-cell operation. (a) Two-Vth scheme, where the device has two sets of Vth. (b) Four-Vth scheme, where the device has four distinct Vth's.

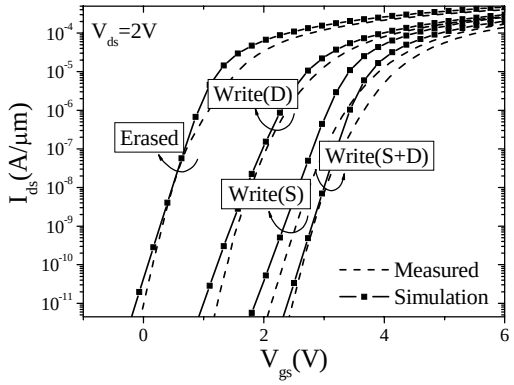

Fig 3. Measured IV characteristics of SNM with the four-Vth scheme. Lg = 0.22 μm, Program voltage is 6V, and program time is 100ms. Simulation data are also shown, where we assume that t_{ox} = 25nm, , x_j = 140nm, N_A=1x10^{17}, charge density is 2.7x10^{12}, and the fraction on of charged NCs in the source and drain side is 50%.

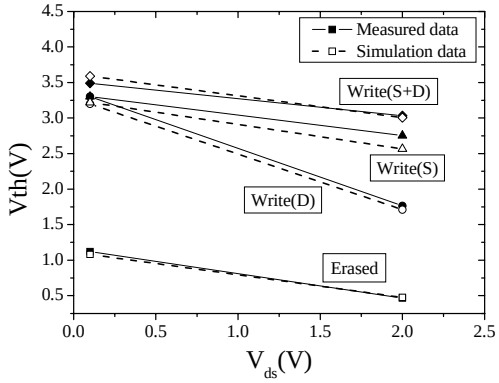

Fig 4. Measured and simulated Vds dependence of Vth in the four states. Lg = 0.22 μm.

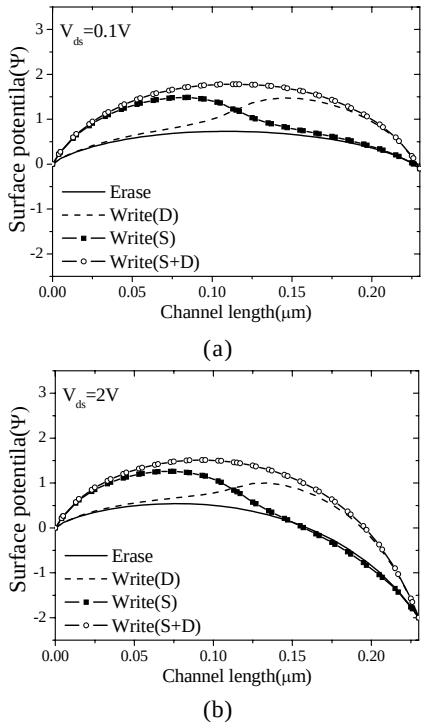

Fig 5. Simulated channel potential profile in the four states of SNM. (a) Vds=0.1V, where Write(D) and Write(S) is symetrical. (b) Vds=2.0V, where larger DIBL takes place in Write(D).

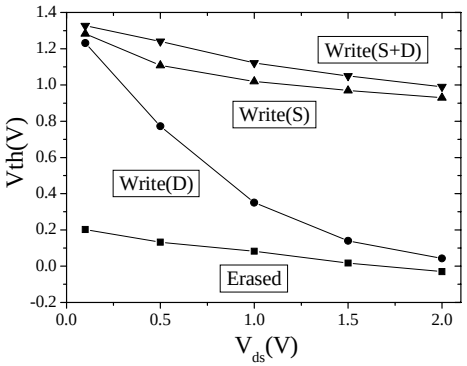

Fig 6. Simulated Vds dependence of Vth in the four states at Lg = 0.15μm. Large DIBL takes placed in Write(D) state than that at Lg = 0.22μm (Fig. 4) . Assured parameters are t_{ox} = 10nm, , x_j = 60nm, N_A=1x10^{17}, charge density is 8x10^{12}, and the fraction on of charged NCs in the source and drain side is 25%.