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ADC and DAC Circuits Using Single Electron and MOS transistors

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1. Introduction

Data conversion between analog signal and digital signal is necessary in modern signal processing system. Progress in LSI technology drives analog-to-digital convertor(ADC) and digital-to-analog convertor(DAC) to develop in direction of high resolution, small area, high speed and low power dissipation. This paper proposes two kinds of novel ADC and DAC hybrid circuits using single electron and MOS transistors.

Some research groups reported ADC and DAC circuits based on single electron tunneling junctions[1-5]. But the load capability and signal swing of the ADC and DAC circuits is too small and their manufacture processes aren't compatible with modern semiconductor micro-fabrication techniques.

This paper proposes two kinds of novel single electron ADC and DAC circuits that consist of single electron transistors (SET), MOS transistors and capacitors. The hybrid ADC and DAC circuits have advantages as follows: 1) large load capability; 2) operate at room temperature; 3) low power dissipation; 4) small area. We simulated the hybrid SET and MOS transistor ADC/DAC circuits. The simulation results demonstrate that the circuits can perform data comversion well at room temperature.

2. ADC and DAC Circuits

Fig. 1 shows schematic of a proposed *n*-bit ADC circuit. It consists of a sampling and holding (S/H) circuit, a signal divider and *n* ADC units. The input signal is inputted to S/H first and then is divided by the divider into *n* signals whose amplitudes are weighted by factors 2^0:2^1:…:2^{n-1}, respectively. Finally *n* signals are converted into digital signals by *n* ADC units. The ADC unit is a hybrid SET and MOS transistor circuit and shows periodic dependence of output voltage on input voltage[6]. We use additional gate and voltage V_S to control the phase of the periodic oscillation and to realize A/D conversion. The periodic output characteristic makes the ADC circuit simple.

Fig. 2 shows the schematic of the *n*-bit DAC circuit that consists of input capacitor array and output circuit. The capacitors with values 2^0C, 2^1C, 2^2C,…$2^{n-1}C$ constitute an input capacitor array. Digital signals are applied to the capacitor array directly. The output is feed backed directly to input in the output circuit that consists of a current source, SET and MOS transistors. If the current of current source is set between maximum value and minimum value of the oscillation current I_{ds} of SET, we can get stable output voltages corresponding to input digital signals. A capacitor C_H and a bias V_H are used to control the range of the output voltage.

3. Simulation and Results

We analyzed the ADC and DAC circuits and found that the size of the interconnection between SET and MOS transistor is large enough and serve as a reservoir for SET transistor rather than a Coulomb island. In this case, we can extract macromodel parameters[7] of SET transistor in the ADC and DAC circuits. We used HSPICE to simulate the operation of the hybrid ADC and DAC circuits.

Fig. 3 shows the simulation results of a 4-bit ADC circuit. The sampling frequency is 12.5 MHz. We took the reference voltage V_{ref} is $V_{DD}/2$. When the analog input signal increases from V_{ref}-0.5V to V_{ref}+0.5V as shown in Fig. 3(a), four digital outputs D_1, D_2, D_3 and D_4 are shown in Fig. 3(b), (c), (d) and (e), respectively. The results show that the circuit can perform A/D conversion at room temperature. The integral nonlinearity (INL) and differential nonlinearity (DNL) of 4 bits ADC circuit are ± 0.1488LSB and ± 0.1692LSB, respectively. The maximum gain error is 0.4%.

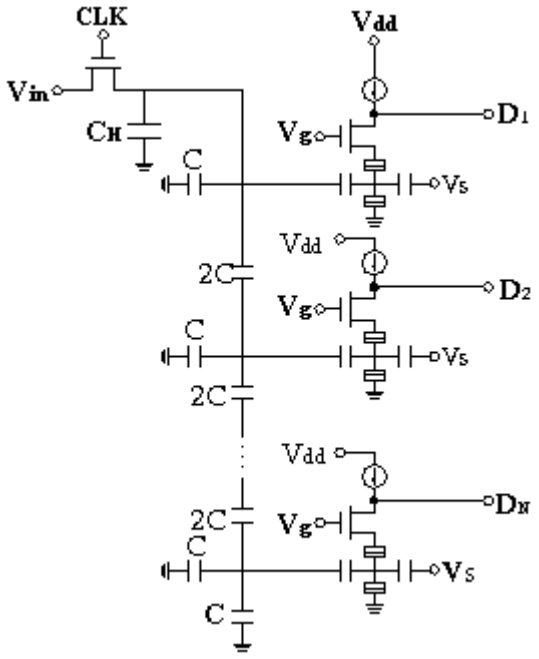

Fig. 1 Schematic of *n*-bit hybrid SET and MOS ADC circuit.

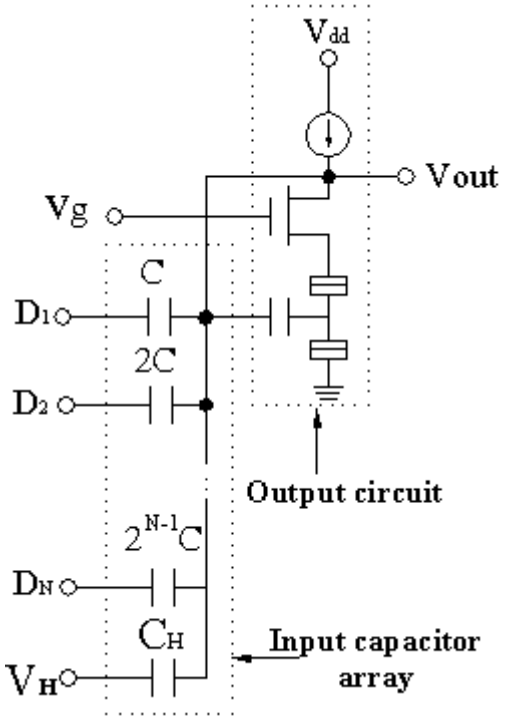

Fig. 2. Schematic of *n*-bit hybrid SET and MOS DAC circuit.

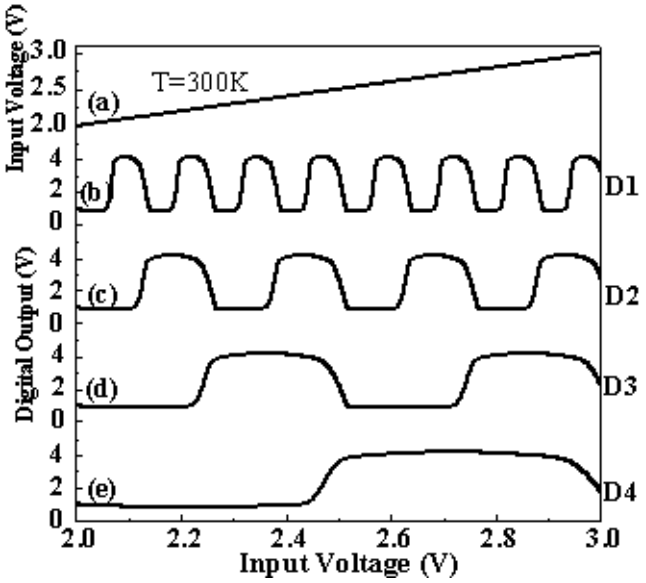

Fig. 3 The simulation results of the 4-bit hybrid SET and MOS ADC circuit.

Fig. 4 shows the simulation results of 3-bit DAC circuit. Fig. 4 (a), (b) and (c) show the digital input signals D_1, D_2 and D_3, respectively. Analog output voltage ranges from 2 to 3V, as shown in Fig. (d). The simulation results indicate that the 3 bits DAC circuits can operate well at room temperature. The INL and DNL of 3 bits DAC circuit are $\pm$ 0.065LSB and $\pm$0.068 LSB, respectively. The maximum gain error is 0.36%.

We analyzed the sampling frequency, power dissipation and resolution of ADC and DAC circuits. The maximum sampling frequencies of ADC and DAC circuit were estimated to be larger than 100MHz and 10GHz, respectively. Their power dissipations of 4-bit ADC and DAC circuits are about 100nW. The highest resolution of the flash ADC and DAC circuits operating at room temperature is 6 bits. In order to realize ADC and DAC with higher resolution, we have to adopt other ADC and DAC architecture, for example pipeline-type ADC.

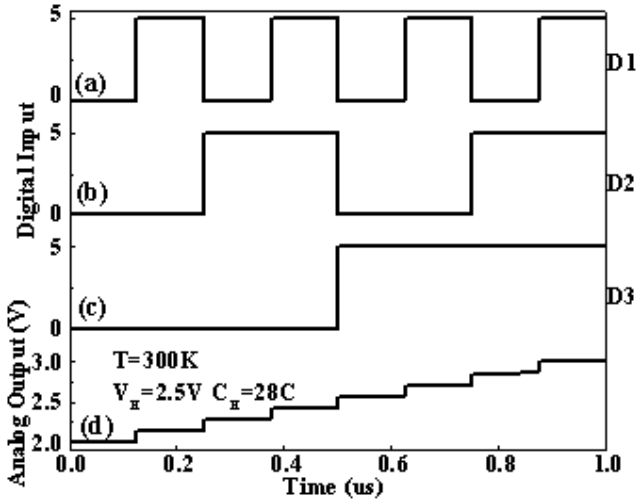

Fig. 4. The simulation results of the 3-bit hybrid SET and MOS DAC circuit.

4.Conclusions

This paper proposes two kinds of novel single electron analog-to-digital (ADC) and digital-to- analog (DAC) converters. The converters consist of single electron transistor (SET), MOS transistor and capacitors. We model the converters using SET SPICE macro-parameters and simulate their operations. The simulation results demonstrate that the converters can operate well at room temperature.

Acknowledgement

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