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P8-6

Strain-Relief Mechanisms of Stepwise Ge composition Multilayer Buffers and High PVCR Si/Si$_{1-x}$Ge$_x$ ASDQW RTD Formed with Triple-Layer Buffer

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1. Introduction

Si/Si$_{1-x}$Ge$_x$ resonant tunneling diodes (RTD) have been intensively studied so far as one of next-generation quantum effect devices fabricated with Si-system material. We have first applied a combination of electron tunneling and multiple quantum wells using a type II band offset structure, and have reported a high peak-to-valley ratio (PVCR) RTD with a PVCR value of ~8 [1].

To realize the type II band offset quantum well structure, we have to first grow a strain-relief relaxed Si$_{1-x}$Ge$_x$ buffer on Si(001) which often causes threading dislocations up to 10^{12} cm^{-2} on the buffer surface which results in a degradation in the RTD *I-V* characteristics. A thick Si$_{1-x}$Ge$_x$ graded buffer with x being varied by 0.1 μm^{-1} has been often used and the dislocation density is reduced to < 10^6 cm^{-2}.

We have investigated the control method for the generation positions of misfit dislocations, and have proposed a thin double-layer buffer with x being stepwise increased and a total thickness of < 200 nm. This buffer has a good crystalline surface with a dislocation density of 10^4 to 10^5 cm^{-2}. The PVCR of an RTD device with this buffer increases to ~180 [2,3].

On the basis of the results on the thin double-layer buffer. We have further advanced the buffer to a triple-layer buffer by insertion of an ultra-thin high Ge content Si$_{1-y}$Ge$_y$ layer between a Si substrate and the double-layer. In this paper, we report the results of a further investigation on the strain-relief mechanisms of these stepwise multi-layer buffer. An RTD device with the triple-layer buffer exhibits PVCR values of 20000 – 50000 which are far larger than those of general III-V RTDs.

2. Experimental

Undoped Si$_{1-x}$Ge$_x$ layer were grown on 0.8-1.2 Ω-cm n-type Si(001) by gas-source molecular beam epitaxy in an ultra-high vacuum system with a base pressure of ~5 x 10^{-10} Torr using GeH$_4$ and Si$_2$H$_6$ for Ge and Si, respectively. The growth temperatures were 600 – 630 ºC.

3. Results and Discussion

Relaxation of Single Si$_{1-x}$Ge$_x$ layer on Si(001)

The relaxation rate and threading dislocation density dependence of a single Si$_{0.82}$Ge$_{0.18}$ layer on Si(001) on its thickness is shown in Fig. 1. When the thickness is 200 nm, the layer is completely coherently grown and the relaxation rate is 0 %. The critical thickness is between 200 and 300 nm in our system. When the thickness is 400nm, the layer is relaxed by 32 % and the dislocation density is ~2 x 10^8 cm^{-2}.

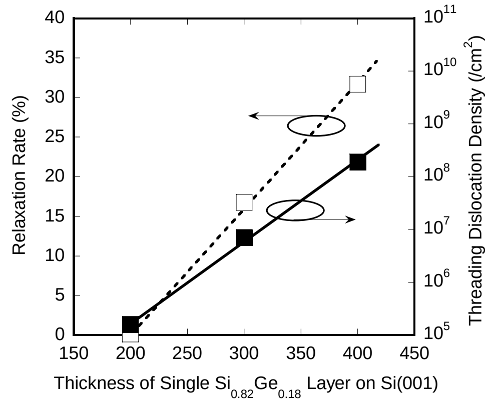

Fig. 1. Relaxation rate and threading dislocation density dependence of a single Si$_{0.82}$Ge$_{0.18}$ layer on Si(001) on its thickness.

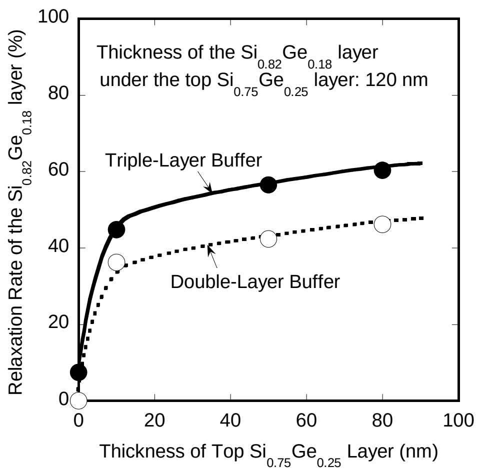

Fig. 2. Relaxation rate dependence of the lower Si$_{0.82}$Ge$_{0.18}$ layer on the thickness of the top Si$_{0.75}$Ge$_{0.25}$ layer of the double-layer and triple-layer buffers.

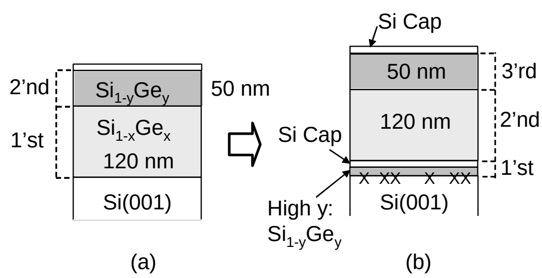

Fig.3. Schematic of (a) a stepwise thin double-layer buffer and (b) a triple-layer buffer where high Ge composition ultra-thin layer is inserted under the thin double-layer buffer.

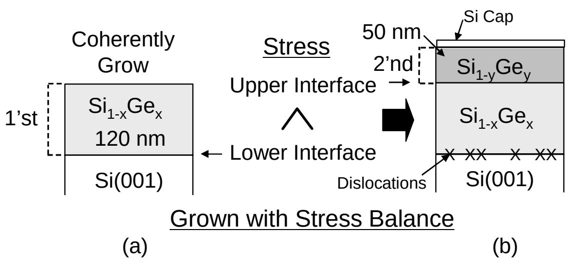

Fig. 4. Strain-relief mechanisms of the double-layer buffer.

Relaxation of Double- and Triple-Layer Buffer

In the double-layer buffer, the $Si_{0.82}Ge_{0.18}$ layer was grown as the 1'st layer (lower layer). The thickness of the 1'st layer was set to 120 nm which is near half a critical thickness. When the 2'nd $Si_{0.75}Ge_{0.25}$ layer was grown, the 1'st layer was relaxed by only 10-nm thick 2'nd layer growth as indicated by dashed line in Fig.2. The relaxation rate exhibits the saturation behavior and the relaxation rate was ~42 % when the 2'nd layer thickness was 50 nm. And this double-layer structure is illustrated in Fig.3(a). The threading dislocation density was in the order of 10^4 to ~2 x 10^5 cm^{-2} which is far lower than that for thick single layer growth as shown in Fig.1. The lattice mismatch was ~0.32 % for the lower interface and ~0.042 % for the upper interface. These results indicate that misfit dislocations are mainly generated in the lower interface and the 2'nd layer prevents the threading dislocations from propagating to the top surface. These strain-relief mechanisms are modeled in Fig.4.

In order to concentrate misfit dislocations into the lower interface and to obtain the stable dislocation position control, we have further advanced the double-layer buffer to a triple-layer buffer by insertion of an ultra-thin high Ge content SiGe alloy layer between a Si(001) substrate and the double-layer as illustrated in Fig.3(b). The Ge composition of the ultra-thin high Ge content layer (1'st layer) was set at the same as that of the top $Si_{0.75}Ge_{0.25}$ layer, and its thickness was set to ~8 nm which is near the border of critical thickness calculated by Matthews and Blakeslee [4]. To prevent threading dislocations from directly propagating to the upper 2'nd layer, an ultra-thin Si layer with a thickness of 5 nm is inserted between the 1'st and 2'nd layers.

The relaxation dependence of the triple-layer buffer on the thickness of the top $Si_{0.75}Ge_{0.25}$ is also shown by solid line in Fig. 2. Before the top layer growth, the relaxation rate was ~7 %. The relaxation behavior is basically the same as that for the double-layer buffer. The relaxation rate was increased by 15 % by the ultra-thin layer insertion. The very-thin top layer growth causes the lower layer relaxation. The results of lattice mismatch measurements also indicates the concentration of misfit dislocations in the lower interface. The dislocation density was in the range of < 2 x 10^5 cm^{-2}.

ASDQW RTD Performance with Triple-Layer buffer

Asymmetric double quantum well (ASDQW) RTD formed with the triple-layer buffer was fabricated. The structure and *I-V* characteristics are shown in Fig. 5 and 6, respectively. Very low background currents and very high PVCR values of 20000 to 50000 were obtained, indicating that the buffer surface crystallinity is high enough. The fact, in turn, clears that inelastic scattering in Si/ $Si_{1-x}Ge_x$ RTD is inherently very low.

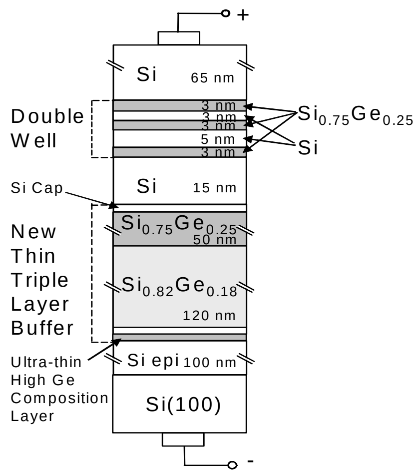

Fig. 5. Structures of an asymmetric double-quantum-well RTD formed with the triple-layer buffer.

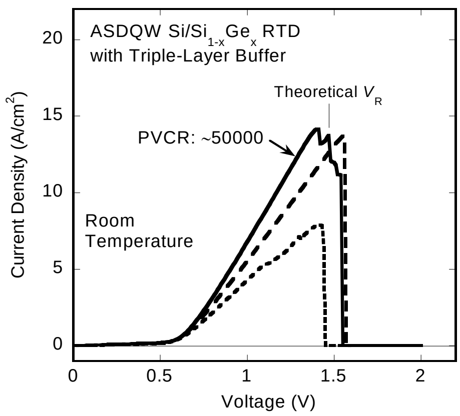

Fig. 6 *I-V* characteristics obtained with the RTDs corresponding to Fig. 5. PVCR ratios of 20000 to 50000 were obtained, which indicates inherently very low inelastic scattering in $Si/Si_{1-x}Ge_x$ RTDs.

4. Conclusions

We have investigated the strain-relief mechanisms of thin double-layer and triple-layer buffers. In this structure system, very thin top layer relaxes the lower SiGe alloy layer. Misfit dislocations mainly concentrate in the lower interface and the top layer prevents threading dislocations from propagating to the top buffer surface. ASDQW RTD exhibits high static performance with PVCR values of 20000 to 50000 which is far larger than those of general III-V RTDs, indicating good crystallinity and very low inelastic scattering in Si/ $Si_{1-x}Ge_x$ quantum well devices.

References

[1] Y. Suda and H. Koyama, Appl. Phys. Lett. **79**, 2273 (2001).
[2] S. Yamaguchi, A. Meguro, and Y. Suda, Ext. Abs. Int. Conf. Solid State Devices and Materials (Japan Society of Applied Physics, Tokyo, 2001) p.58.
[3] Y. Suda, ECS Proc. Volume on Advanced Luminescent Materials and Quantum Confinement II, ed. by M. Cahay et. al (The Electrochemical Society Inc., NJ, 2002) p. 47.
[4] J. W. Matthews and A. E. Blakeslee, J. Cryst. Growth **27**, 118 (1974).