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Two-Dimensional Quantum Mechanical Modeling of Strained-Si FinFETs on SiGe-On-Insulator(SGOI)

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1. Introduction

As critical device features begin to approach 100nm, there are certain impediments like short channel effects (SCE), oxide and silicon tunneling, difficulty in lithographic patterning, etc [1]. Double-gate (DG) MOSFET structures can overcome these limitations to transistor scaling [1]. Among DG MOS devices, the FinFET is considered to be the most promising candidate due to its simple process [2]. Meanwhile, the sub-100nm MOSFETs with a high mobility channel using strained Si are currently stirring a strong interest as high performance and low power CMOS device structures owing to the suppression of intervalley scattering and the low in-plane conduction mass by the biaxial tensile strain [3,4], and the velocity overshoot effect [5,6].

Implementing strained Si (SS) fin on SiGe-on-insulator (SGOI) structure, the strained Si FinFET (SSFinFET) may have the potential to combine the advantages of strained Si and FinFETs. A strained Si fin can be fabricated by using wafer bonding, SIMOX, or Ge condensation process like SS on SGOI [4]. In order to optimize the structure of SSFinFET, it is necessary to undertake a two-dimensional (2-D) quantum mechanical simulation because of its inherent quantum and geometrical effects on the electronic properties of nanoscale semiconductor devices. It should be also considered the changes of the effective mass, mobility, and occupied valley by a strain.

In this study, we have discussed SCE as well as I-V characteristics for SSFinFETs and relaxed Si FinFETs (RSFinFETs). To do so, we have used 2-D Schrödinger and Poisson equation in a self-consistent manner.

2. Device Structure

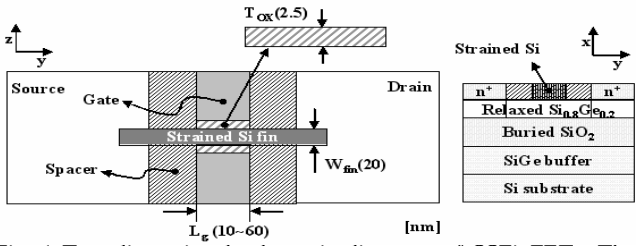

Fig. 1 Two-dimensional schematic diagrams of SSFinFETs. The channel is the strained Si fin.

Figure 1 shows the schematic diagrams of the SSFinFETs. The channel is the strained Si grown on the relaxed $Si_{0.8}Ge_{0.2}$-on-insulator. Two symmetric metal gates with workfunction Φ_M =4.1eV are located on both side of the strained Si fin. The source and drain regions are modeled as ohmic contacts with a doping of $1\times10^{20}cm^{-3}$, and under the gate doping is $1\times10^{15}cm^{-3}$. The gate length (L_g) is varying in a range (10–60 nm), while fin width (W_{fin}) is fixed to 20nm.

3. Numerical Model

The 2-D quantum mechanical model used for the description of bound states in a region where the confinement for electrons is strong in both y and z direction. The three main equations, nonlinear Poisson equation for electrostatic potential (Φ), 2-D Schrödinger equation, and current continuity equation are written as

$$div(\varepsilon\nabla\Phi) = q(n - p + N_A^- - N_D^+), \quad (1)$$

$$\left(-\frac{\hbar^2}{2m_y^\nu}\frac{\partial^2}{\partial y^2} - \frac{\hbar^2}{2m_z^\nu}\frac{\partial^2}{\partial z^2} + V\right)\phi_n^\nu = E_n^\nu\phi_n^\nu, \quad (2)$$

$$div\vec{j}_n = div(n\mu_n\nabla E_{Fn}) = 0, \quad (3)$$

where ε is the dielectric constant, q the unit electric charge, n and p electron and hole concentrations considering the energy eignestates and the corresponding eigenfuncions, N_D^+ and N_A^- ionized donor and acceptor concentrations calculated using statistical mechanics of impurity, m_i^ν the effective mass in i direction considering each equivalent three ellipsoidal valley pair ν in Si, V the potential energy, ϕ_n^ν the wavefunction of the nth eigenstates in ν valley belonging to energy level E_n, j_n the electron current density, μ_n the electron mobility, E_{Fn} the quasi-Fermi level. Here μ_n in the low and high field used the modified empirical-fit relationship considering the strain and velocity overshoot effects on electron mobility in strained Si channel [3,5,6].

4. Results

Figure 2 shows the I_d-V_d characteristics for SSFinFETs and RSFinFETs with L_g=30nm and W_{fin}=20nm at V_g=0.25 and 0.5V. Over 25% I_{dsat} enhancement is observed due to the electron mobility improvement and the more velocity overshoot in strained Si. In conduction band, the energy splitting due to the biaxial tensile strain suppresses intervalley carrier scattering between the two-fold and four-fold

degenerate valleys, and causes preferential occupation of the two-fold valleys where the in-plane conduction mass is lower. These two effects lead to increase the low field electron mobility [3]. In addition, the reduction of intervalley scattering rates increases the energy relaxation times as well as the difference between the momentum- and energy-relaxation times as the Ge mole fraction [5,6]. This occurrence produces an enhancement of the electron velocity overshoot effects in theses devices.

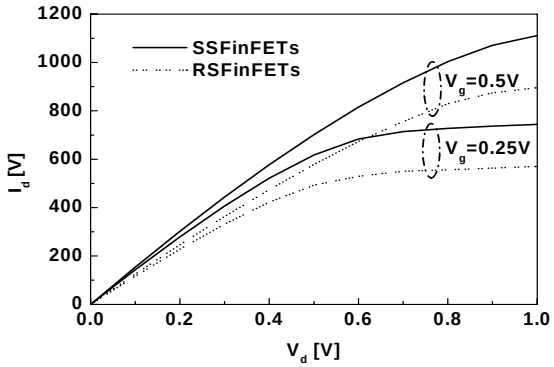

Fig. 2 I_d-V_d characteristics for SSFinFET and RSFinFETs with W_{fin}=20nm and L_g=30nm at V_g=0.25 and 0.5V.

Figure 3 shows I_d-V_g characteristics with W_{fin}=20nm at V_d=0.1V for SSFinFETs while L_g is varying from 10 to 60 nm. It is noted that the threshold voltage (V_T) becomes smaller and subthreshold swing becomes larger as L_g is decreased.

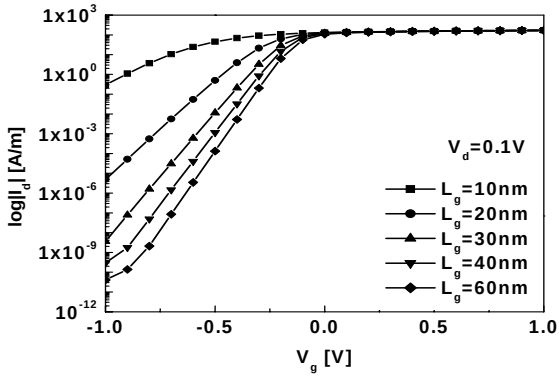

Fig. 3 I_d-V_g characteristics for SSFinFETs with W_{fin} of 20nm and L_g of 10-60nm at V_d=0.1V.

V_T and subthreshold swing characteristics as a function of L_g for the devices are shown in Figure 4. The steepness of the V_T roll-off and subthreshold swing for the SSFinFETs are found to be similar to those of the RSFinFETs because there is no difference in the electronic conduction band offset between two cases. Also, the results show that adequate suppression of SCE requires that the ratio of L_g to W_{fin} is larger than about 1.5 [7]. Drain induced barrier lowering (DIBL) as a function of L_g for the devices are shown in Figure 5. As shown Figure 4, when the L_g be approximately 1.5*W_{fin}, the DIBL are below 0.1V/V.

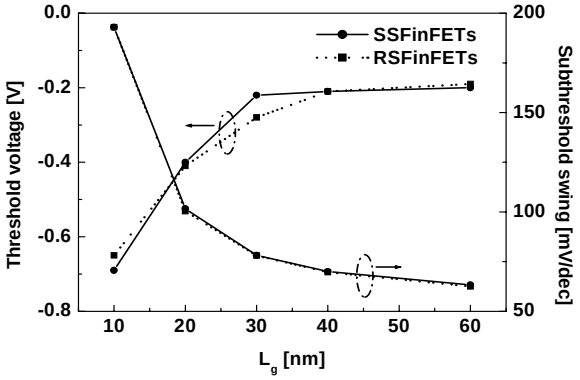

Fig. 4 V_T and subthreshold swing characteristics for SSFinFETs and RSFinFETs with W_{fin}=20nm as a function of L_g.

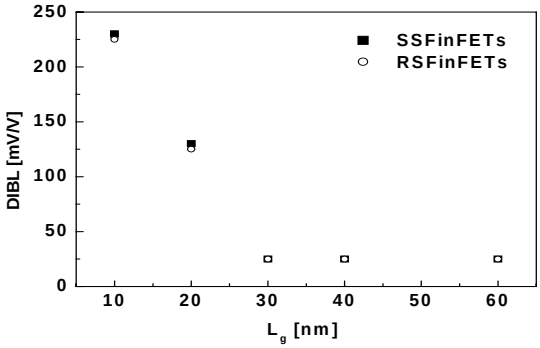

Fig. 5 DIBL for SSFinFETs and RSFinFETs with W_{fin}=20nm as a function of L_g.

5. Conclusions

In strained-Si FinFETs on SiGe-on-insulator, the drain current was found to be enhanced by up to 25% compared with the conventional FinFET due to the strain and velocity overshoot effects. However, similar short channel effects (SCE) and drain induced barrier lowering (DIBL) behaviors are shown whether a strain is or not. The adequate suppression of SCE and DIBL requires that the L_g be approximately 1.5*W_{fin}.

Acknowledgements

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References

[1] S. J. Wind, D. J. Frank, and H. -S. Wong, Microelectronic Engineering, **32** (1996) 271.

[2] D. Hisamoto et al, IEEE Trans. Electron Devices, **47** (2000) 2320.

[3] F. M. Bufler and W. Fichtner, Appl. Phys. Lett. **81** (2002) 82.

[4] K. Rim et al, Solid-State Electronics **47** (2003) 1133.

[5] J. B. Roldan, R. Gamiz, J. A. Lopez-Villanueva, and J. E. Carceller, IEEE Trans. Electron Devices, **45** (1998) 993.

[6] F. M. Bufler and W. Fichtner, IEEE Trans. Electron Devices, **50** (2003) 278.

[7] X. Huang et al, *International Electron Devices Meeting* (1999) 67.