Extended Abstracts of the 2004 International Conference on Solid State Devices and Materials, Tokyo, 2004, pp. 4-5

PL-2 (Plenary)

Silicon-based Devices and Technology for the Nanoscale Era

James D. Plummer

Center For Integrated Systems, Stanford University, Stanford CA.
Phone: 650 723-3938, Email: plummer@ee.stanford.edu,

1. Introduction

For more than 40 years silicon technology has followed Moore's Law, increasing chip complexity, decreasing device dimensions and increasing device speed. The apparent ease with which all this has happened, has led to an expectation that faster and more powerful chips will continue to be introduced on the same schedule for the foreseeable future. In fact the ITRS now extends this device scaling and increased functionality scenario for at least another decade, at which point, minimum feature sizes are projected to be below 20 nm.

Most of the history of the past 40 years has been achieved with the same basic switching element (the MOS transistor), the same basic circuit topology (CMOS) and with a limited number of materials (Si, SiO_2, Al, Cu, Si_3N_4, $TiSi_2$, $CoSi_2$, TiN, and W primarily). While very substantial human and financial resources have been invested in scaling dimensions and increasing chip sizes, in many respects progress in these areas has been straightforward in the sense that no fundamentally new inventions have been needed.

2. The Next 10 Years

Because we are now approaching a number of more fundamental limits in technology and device performance, the rate of introduction of new technologies and new device structures will certainly increase in the next decade. Limits on scaling SiO_2 thickness have led to oxynitride gate dielectrics and will soon lead to high K gate materials. Limits on active dopant concentrations achievable by implantation and RTA have led to flash annealing methods and the resulting metastable dopant concentrations. Strained silicon active device layers are being introduced because of the higher carrier mobilities achievable in this material. New semiconductor materials like SiGe have been introduced for heterojunction bipolar transistors and even pure Ge is being seriously considered for MOSFET channel regions, again because of higher carrier mobilities. New gate electrode materials like SiGe and even metals are now serious contenders for future scaled device structures.

As device structures have been scaled, control of electrostatics in small devices (good short channel performance), has led to SOI technologies and to proposals for double-gate, tri-gate or Finfet structures and various vertical MOSFET devices. SOI is already a mainstream technology. Some of the others will certainly become mainstream within the next decade. Variations of the Finfet structure will likely be the first to be widely used in mainstream technology, because these structures are most compatible with standard planar technology. But all of these proposed devices are basically modified MOSFETs. They provide better short channel control, higher drive currents and compatibility with standard circuit design techniques and system architectures.

The list of possible materials and device structure innovations in the next decade could go on. The most likely scenario that will almost certainly hold, is that the MOSFET device and CMOS based circuits will be the only major players in this time frame. However, for really the first time in the history of silicon chip technology, we are seeing and will see over the next decade, real changes in the breadth of materials used to build silicon chips and real changes in the basic planar MOSFET device structure.

3. Beyond Simple Scaling

If history is any guide, the next 10 years will produce many new device and technology ideas that potentially can replace or supercede MOSFETs and CMOS circuits. If history is any guide, most of these will not find widespread application in mainstream silicon chip

technology. Those that do have a major impact will do so because they solve a major problem that is not easily solved by simple scaling, circuit design or new chip architectures. Given the tremendous investment in standard CMOS technology any alternatives must offer major improvements if they are to have any significant impact. A number of such alternatives will be discussed in this presentation. Typical examples are shown below.

Fig. 1 illustrates the IMOS device concept that achieves subthreshold slopes much steeper than the kT/q limit (60 mV/decade) achieved by MOS devices. The device operates by using MOS gated avalanche breakdown in a PIN diode structure. Devices like this potentially make possible reduced supply voltage and reduced static power dissipation in chips. Because the device relies on hot carriers for its basic operation, reliability issues associated with charge trapping in dielectrics are an important issue.

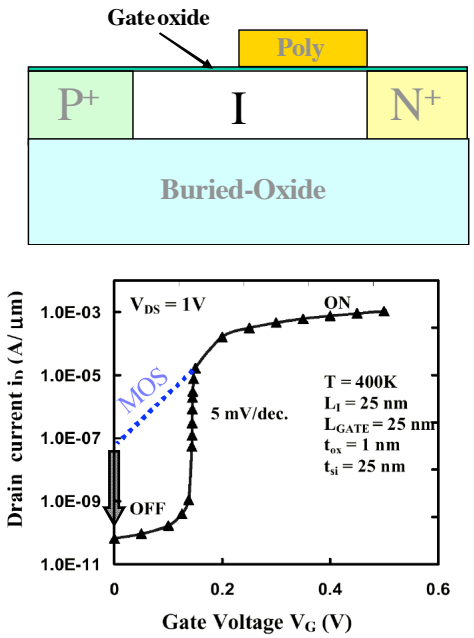

Fig. 1: IMOS device and simulated abrupt subthreshold slope [1].

Many proposals have been made for "3D" integration in silicon technology. To date, the impact has largely been in backend processing where many layers of interconnect can now be easily incorporated in chips. Interconnect layers require only two masks per wiring level and only low temperature materials.

3D integration of active device layers has not been nearly as successful because stacking high quality single crystal semiconductor layers has proven very difficult, and because forming active device layers typically requires 10 to 20 mask layers for each active device layer. True 3D stacking of active devices will likely require materials innovation to achieve high quality single crystal stacked layers, and device innovation so a reasonable mask count can be used per active layer.

Fig. 2 illustrates one step in this direction using liquid phase epi to produce single crystal Ge on insulator layers on Si substrates, potentially allowing heterogeneous integration of devices in different materials.

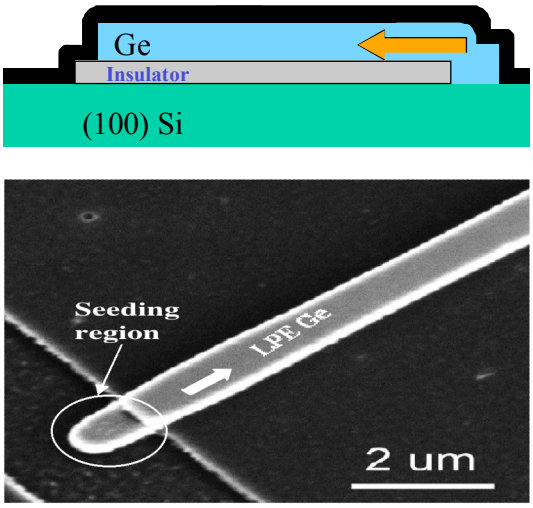

Fig. 2: LPE Ge technology [2].

4. Conclusions

The silicon semiconductor industry has charted a course for itself over the next 15 years, which basically continues the density and performance improvements of the past 40 years. There do not appear to be many, if any, "fundamental" roadblocks that will prevent this from actually occurring. Nevertheless, these future technology generations will not happen as easily as past generations have. Significant materials and device innovation will have to occur beyond simple scaling.

[1]. K. Gopalakrishnan, P. B. Griffin and J. D. Plummer, "I-MOS: A Novel Semiconductor Device with a Subthreshold Slope Lower Than kT/q", IEDM, Paper 11.3, Dec. 2002.
[2]. Y. Liu, M. Deal and J. D. Plummer, "High Quality Single-crystal GeOI by Liquid-phase Epitaxy on Si Substrates", Appl. Phys. Letters, Vol. 84 No. 14, pg. 2563, April 2004.