Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.6-7

A-1-1 (Invited)

Current Status and Addressing the Challenges of Hf-based Gate Stack toward 45nm-LSTP Application

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1. Introduction

In spite of intensive efforts, still some serious items to be solved remain for high-k gate stack. By narrowing down the items, gate electrode has become one of the most problematic issues due to unavoidable Fermi level pinning [1]. In this talk, after a brief benchmarking of high-k gate stack technology, we lay particular stress on the impact on the electrical characteristics concerning the gate electrodes [poly Si and metal gate including fully-silicided(FUSI) gate] and interfacial reaction control [post deposition anneal(PDA) and nitride capping] as well as Hf-based high-k dielectric material.

2. Results and discussions

Poly Si, Ni-FUSI gated MOS FETs down to L_g = 50nm with (SiN)/HfO_2,HfSiON/SiO_2 were fabricated by a conventional self-aligned process.(Fig.1) As for the Hf-based high-k dielectric, apart from reliability issue, each formation method in general makes little difference in the electrical performance when the method and FET fabrication process are sufficiently optimized.

Owing to its high C_{inv} and low EOT, Hf based gate stack with FUSI has become one of the promising candidate for 45nm-LSTP application. Among them, Ni-FUSI is intensively investigated recently [2, 3]. However, the FUSI gate brings about worse yield across the wafer [4] and can be effective only if it is prepared under certain conditions [5]. Also, SiN capping on HfO_2 can act as a protective layer leading higher transistor yield, however, as shown in Fig.2, it cannot suppress a scatter in the I_{on}-I_{off} characteristics. Compared with Poly Si gated FETs, this trend also happened for the FUSI/SiN/HfO_2/SiO_2-FETs.(not shown) However, when an elevated PDA temperature treatment is introduced, this problematic scattering has been found to be drastically reduced(Fig.3). This implies reaction-related roughness or defects at upper interface between Ni-FUSI and HfO_2 is a main cause of the electrical degradation. This is also confirmed by other experiments including V_t-L_g, J_g-V_g. Control of the upper interfacial reaction is a key issue for FUSI/high-k stacks.

By these treatments, excellent performance was obtained for the Ni-FUSI/SiN/HfO_2/SiO_2/Si system, i.e., I_{on} (n/p) = 600/180 uA/um with I_{off} =20 pA/um at V_{dd}=1.1V.

On the other, different from the HfO_2, NH_3 treatment plays a role of the SiN capping for Hf-silicate, since Si-N bonds rather than Hf-N can easily be formed in the $HfSiO_x$. In case of the FUSI/HfSiON stacks with optimized NH_3 annealing, the scatter in the electrical characteristics is improved. This means the nitrided surface on the $HfSiO_x$ is capable of protecting from the interfacial reaction. In addition, different from HfO_2, Hf-silicate stays amorphous with less reaction with Si in the gate even after high temperature annealing(>1000C). [6] Strategically, in spite of its lower k value than HfO_2, the use of HfSiON with Ni-FUSI gate is worthwhile due to its EOT scalability and less gate leakage.

Concerning FUSI potentiality, from process controllability point of view, variety of silicide phases can be produced in the gate due to narrowing effect of the gate [2]. Darker contrast in the XTEM image in Fig. 4 indicates a Ni-rich regime, conversely brighter contrast for a less Ni regime. Since each phase has respective work function, the phase control is primary important. Due to the work function difference, as shown for the pMOS case in Fig.5-6, Ni-rich gate can provide lower V_t, hence high drivability, while NiSi gate provides higher V_t with poor drivability as indicated by (b) and (a) respectively. We recently confirmed this occasional phase separation could be controllable. This presents a rosy picture. CMOS integration with wide process window are needed in addition to further material research towards potential band-edge (FUSI) gate. Since it may give different aspects, reliability study is requisite.

3. Conclusion

As far as performances are concerned, by suppressing the interfacial reaction between high-k and gate electrode and controlling the phase in the Ni silicide gate, Ni-FUSI/ HfSiON gate stack can be promising candidate for 45nm-LSTP MOSFETs. There are pressing needs for its CMOS integration and reliability confirmation.

Acknowledgements
Authors would like to thank Dr. A. Lauwers and Dr. J. A. Kittle at IMEC for their FUSI technology.

References
[1] C. Hobbs et al., Symp. on VLSI Technology, p.9, (2003).
[2] J. A. Kittle et al., Symp. on VLSI Technology, p.72, (2005).
[3] S. Kubicek et al., Symp. on VLSI-TSA, p.99, (2005).
[4] C. S. Park et al., IEDM Tech. Digest, p299, (2004).
[5] R. Mitsuhashi et al., Proc. of INFOS, p7 (2005).
[6] K. Yamamoto et al., Proc. of INFOS, p198 (2005).

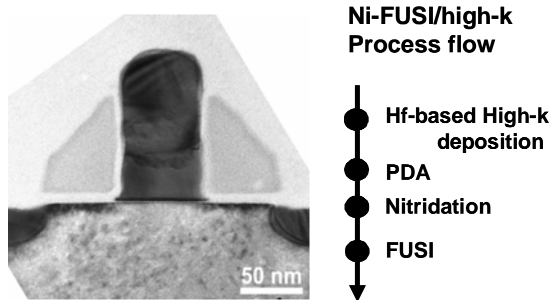

Fig. 1 XTEM of Ni-FUSI gated Hf-based transistor.

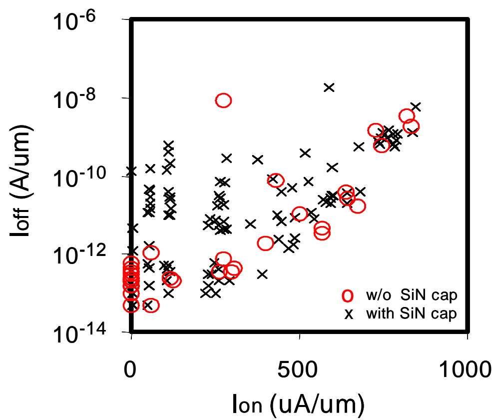

Fig. 2 Influence of SiN capping on I_{on}-I_{off} characteristics of FUSI/HfO_2 for nMOS. FETs with SiN cap show better yield but with spread I_{off} values than those without SiN cap.

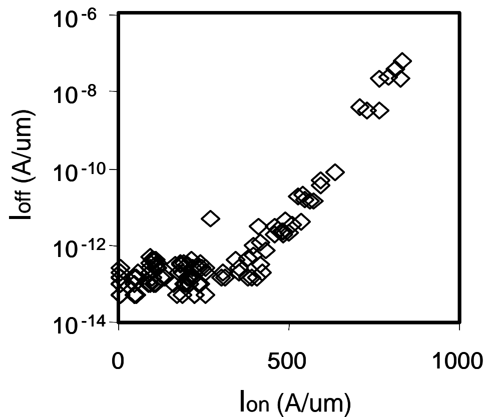

Fig. 3 I_{on}-I_{off} of FUSI/SiN/HfO_2 for nMOS after optimized post deposition anneal(PDA). By suppressing the interfacial reaction, excellent drivability is obtained.

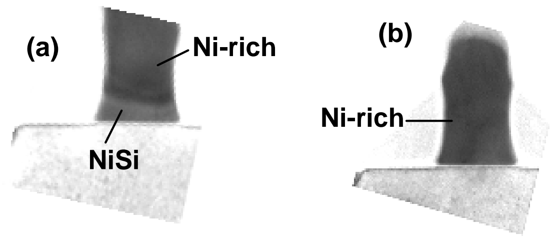

Fig. 4 XTEM of Ni-FUSI/SiN/HfO_2 for pMOS. (a) indicates less Ni phase near the interface and Ni-rich at upper area in the FUSI gate, and Ni-rich phase in the gate for (b). Darker contrast corresponds to Ni-rich regime.

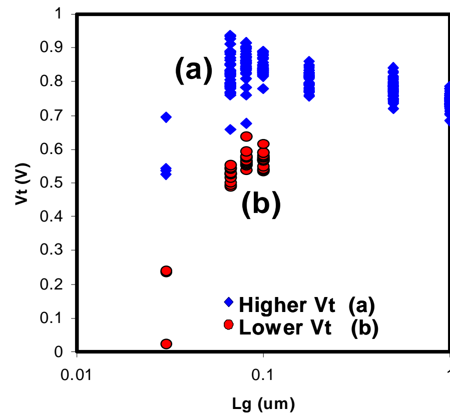

Fig. 5 V_t-L_g of Ni-FUSI for FUSI/SiN/HfO_2 for pMOS indicating less Ni has higher V_t(a) and Ni-rich has lower V_t(b). (a), (b) correspond to those in Fig. 4.

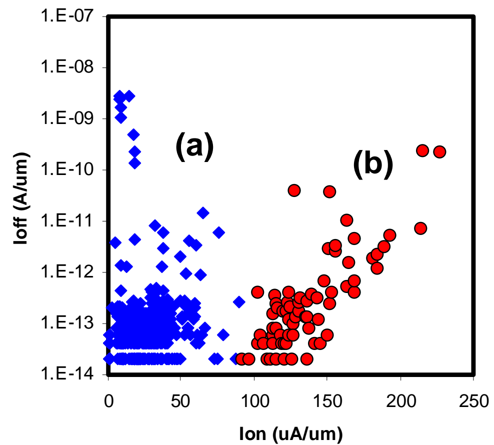

Fig. 6 I_{on}-I_{off} of Ni-FUSI for FUSI/SiN/HfO_2 for pMOS. Higher(Lower) I_{on} corresponds to lower(higher) V_t values. (a), (b) correspond to those in Fig. 4 and 5.