

The Impact of Thickness Control in HfSiON Gate Dielectric on Electron Mobility with sub-nm EOT

M. Mizutani, T. Hayashi, M. Inoue, J. Yugami,¹K. Nomura, J. Tsuchimoto, Y. Ohno, and M. Yoneda
Process Technology Development Div., RENESAS Technology Corp.,

¹Wafer Process Engineering Dept.(1), RENESAS Semiconductor Engineering Corp.,
4-1 Mizuhara, Itami-shi, Hyogo 664-0005 Japan

Phone: +81-72-784-7355, Fax: +81-72-780-2675, e-mail: mizutani.masaharu@renesas.com

1. Introduction

The HfSiON gate dielectric is one of the most promising candidates for replacing conventional SiON in next generation CMOS devices. However, to avoid electron mobility reduction, a relatively thick interface layer (IL) under the HfSiON gate dielectric must be introduced. Thus, it is difficult to reduce the EOT of the HfSiON stack to less than 1nm.

In order to scale down the EOT of the HfSiON gate stack while maintaining high electron mobility, we have studied electron mobility of the HfSiON gate stack with an interface layer (IL) formed by post deposition annealing (PDA). From systematic study of electron mobility varying both HfSiON and IL thickness, we found that the HfSiON/IL stack has higher mobility than SiON under high electric field (~0.8MV/cm) when a high-quality interface layer of sufficient thickness was formed. This electron mobility enhancement should originate in the Hf atoms at the gate electrode interface. On the other hand, the electron mobility was reduced with EOT scaling in both cases, HfSiON thickness reduction and IL thickness reduction. This phenomenon can be explained assuming multiple sources of mobility reduction located at IL, HfSiON, HfSiON/IL interface and gate/HfSiON interface. Moreover, EOT and HfSiON thickness affect gate leakage current and threshold voltage. Thus, precise control of the thickness of both HfSiON and IL is the key to achieving preferable Ion-Ioff characteristics in scaled EOT(<1nm).

As a result of our research, we were able to obtain a HfSiON/IL stack with EOT=0.9nm while maintaining electron mobility as high as 80% of that of thick SiON.

2. Experimental

After isolation formation on (100) Si substrate, various thicknesses of HfSiO were deposited by MOCVD on chemical oxide. The IL thickness was controlled by varying temperature (800~1000°C) and O₂ pressure (54~100kPa) during PDA. After plasma nitridation, a poly-Si gate was formed using LPCVD. To fabricate nFET, dopants in the gate and Source/Drain were activated by spike annealing at 1050°C. The optical thickness of HfSiO films was measured by ellipsometry and the EOT was evaluated using an EPOQUE[1] quantum mechanical C-V simulator. Fig.1 shows the dependence of the HfSiON/IL stack's EOT on HfSiO optical thickness. It suggests that IL thickness is independent of HfSiO thickness. Thus, the EOT of IL was able to be controlled between 0.30 to 0.85nm. The composition depth profile of the HfSiON/IL stack was analyzed by angle resolved XPS.

3. Results and Discussion

Fig.2 shows the depth profile of Hf, Si, O and N atoms in the HfSiON/IL stack with PDA. The depth profile of HfSiON on chemical oxide is also shown for comparison. For the case with PDA, N and Hf atoms keep away from the Si substrate. This low concentration of Hf and N in the interfacial layer may provide good interface quality in HfSiON stacks. Fig.3 shows an example of electron mobility for the HfSiON/IL stack compared to that for SiON. We achieved universal-like characteristics of electron mobility by changing the substrate impurity concentration. In this case, the EOT of HfSiON/IL was 1.5nm, and EOT_IL was also relatively thick. From this figure we found that mobility for HfSiON/IL is lower in a low electric field and is higher in high field than that of SiON. Thus, we will focus on electron mobility under a high electric field, 0.8MV/cm, which corresponds to the operating condition of CMOS.

It is known that gate/dielectric structure (roughness or potential fluctuation) may degrade electron mobility characteristics [2] and

it is also known that HfSiO at gate interface introduce dipole or fixed charge at the interface [3][4]. Thus, we speculate that the mobility characteristic was modified by change of potential distribution at the gate interface caused by a small amount of Hf atoms at the interface. We found that HfSiON/IL has higher mobility than SiON under a high electric field when a high-quality interface layer of sufficient thickness was formed. Unfortunately, electron mobility decreases significantly with EOT scaling as shown in Fig.5. Mobility degradation can also be caused by many scattering sources as shown in Fig.6. Thus the mobility μ_{eff} can be written as $\mu_{eff} \sim (\mu_1^{-1} + \mu_2^{-1} + \mu_3^{-1} + \mu_4^{-1} + \mu_5^{-1})$. Where μ_n represents the mobility restricted by scattering sources located at position n , which is shown in Fig. 6.

To confirm the influence of scattering sources on the mobility, we executed two experiments. The first was a comparison of the mobility of several HfSiON/IL stacks with the same EOT, as shown in Fig. 7. For the case of EOT=1.5nm, the mobility reduced linearly with decreasing EOT_IL independent of PDA conditions. This result suggests that mobility is mainly restricted by scattering sources located at the HfSiON film or at the HfSiON/IL interface. For the case of EOT=0.9nm, the mobility was independent of EOT_IL when EOT_IL is thicker than 0.5nm. This means that the main scattering source of mobility reduction is located at the gate interface in the case of a thinner EOT. The second experiment was a comparison of the mobility of HfSiON/IL stacks with the same EOT_IL. As shown in Fig.8, it is clear that the mobility was mainly determined by total physical thickness of the HfSiON stacks, except in the case in which EOT_IL is 0.3nm. From the results of the above experiments, we can conclude that total physical thickness of HfSiON stacks should be kept as thick as possible to obtain high mobility in the case of thinner EOT. The combination of thick HfSiON and thin IL at least as thick as than 0.5nm is recommended. The thickness of HfSiON and EOT also affect gate leakage current and threshold voltage (Fig. 9, 10). Thus, further precise control of the thickness of both HfSiON film and IL will be required to achieve preferable device performance. As a result, we obtained HfSiON/IL stack with EOT=0.9nm while maintaining electron mobility as high as 80% of that of thick SiON. The Ion-Ioff characteristics (Fig.11) showed that HfSiON stack with EOT=0.9nm will be suitable for 45nm LOP devices.

4. Acknowledgements

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5. Conclusion

HfSiON/IL stack had higher mobility than SiON under high electric field (~0.8MV/cm) when a high-quality interface layer of sufficient thickness was achieved, although the mobility under low electric fields was degraded. Our systematic study of electron mobility varying both HfSiON and IL thicknesses led to finding that the major source of mobility reduction in thinner HfSiON/IL stacks is located at gate/HfSiON interface. Precise control of the thickness of both HfSiON and IL enabled us to obtain HfSiON/IL stack with EOT=0.9nm while maintaining electron mobility.

References

- [1] S. Saito, et al., IEEE EDL vol.23, 6, p348 (2002).
- [2] S. Saito, et al., IDEM Tech Dig., p.797 (2003)
- [3] K. Shiraishi, et al., VLSI Tech Symposium, p108 (2004)
- [4] L.-A. Ragnarsson et al., IEDM Tech. Dig., p.87 (2003).

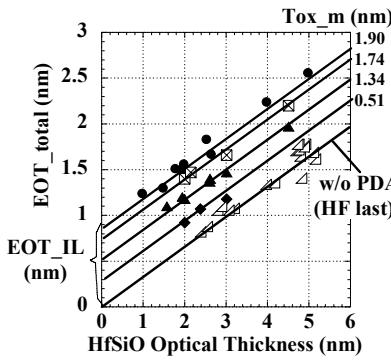


Fig.1 EOT of HfSiO/IL stack vs. HfSiO optical thickness.
Tox_m represents an oxide thickness on Si Substrate with each PDA condition.

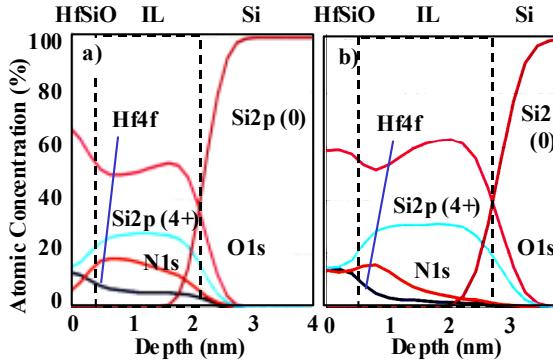


Fig.2 Atomic depth profiles of HfSiON/IL stack calculated by Maximum Entropy Method using data from angle resolved XPS.

a) HfSiON w/o PDA, b) HfSiON with PDA.

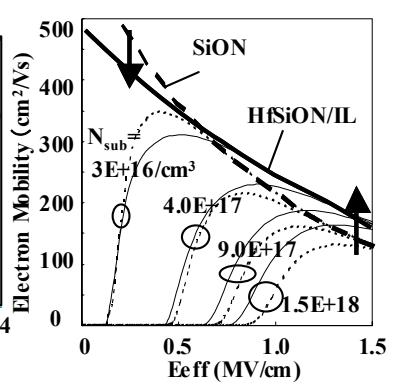


Fig.3 Dependence of electron mobility on substrate impurity concentration.

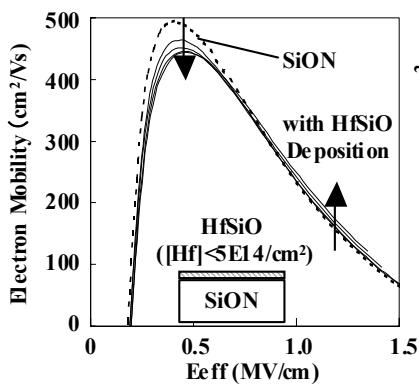


Fig.4 Electron mobility modification with sub-monolayer HfSiO deposited on SiON.

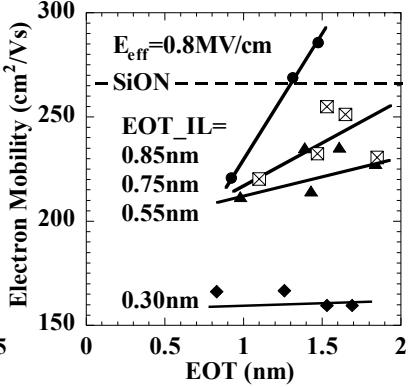
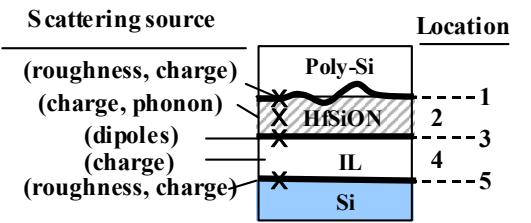


Fig.5 Dependence of electron mobility on EOT.



$$\mu \propto (\mu_1^{-1} + \mu_2^{-1} + \dots + \mu_5^{-1})^{-1}$$

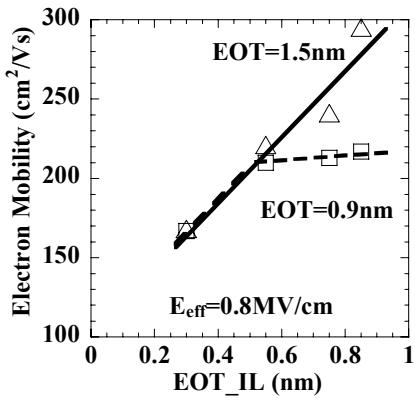


Fig.7 Dependence of electron mobility on EOT_{IL}.

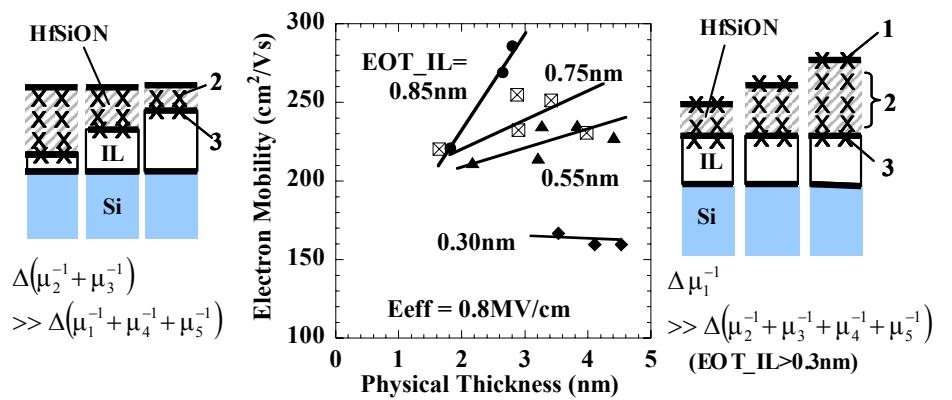


Fig.8 Dependence of electron mobility on total physical thickness of HfSiON/IL stack.

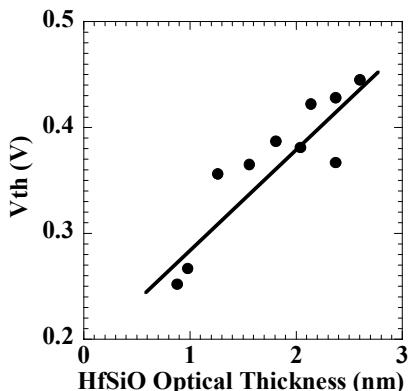


Fig.9 Dependence of threshold voltage, V_{th}, on HfSiO optical thickness.

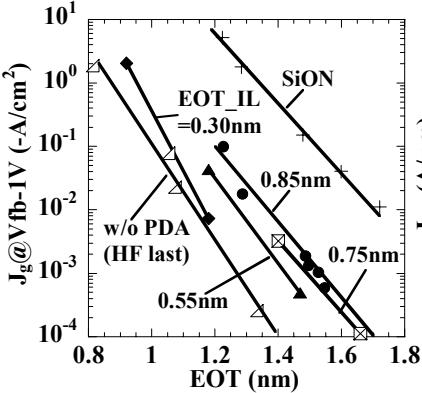


Fig.10 Dependence of leakage current on EOT.

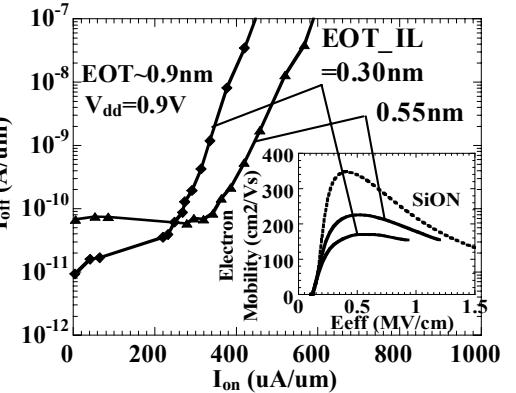


Fig.11 Ion-loff characteristic of nFET. The inset is dependence of electron mobility on Eeff