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Extendibility of High Mobility HfSiON Gate Dielectrics

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1. Introduction

HfSiON is considered the most promising candidate of gate dielectrics for hp65 node LSTP devices due to its high mobility [1-2]. Sub-1nm EOT high-k gate dielectrics are required for LOP devices in hp45 node and beyond [3]. However, the k-value of HfSiON is 16 at most. In order to obtain sub-1nm EOT, the physical thickness of HfSiON must be less than 2nm, even if the interfacial layer thickness is 0.5nm. Such a very small physical thickness causes enormous direct tunneling current. Therefore, the interfacial layer thickness has to be minimized to reduce the leakage current and EOT simultaneously. On the other hand, it is well known that there is a trade-off between carrier mobility and interfacial layer thickness [4].

The objective of this work is to fabricate sub-1nm EOT HfSiON by minimizing the interfacial layer thickness without fatal mobility reduction.

2. Experimental

After interfacial layer formation by ozone oxidation, 2nm-thick HfSiO films were deposited by MOCVD using hafnium tetra-*t*-butoxide (HTB) and disilane (Si_2H_6) as precursors without an oxidizing gas [5]. Post-deposition annealing (PDA) and post-nitridation annealing (PNA) were performed, using a low-pressure rapid thermal processor at temperatures of 600°C to 1050°C. Ar/N_2 plasma nitridation was used to introduce nitrogen into HfSiO films. Radical dominant mode or ion dominant mode plasma was applied [6]. Optical thickness of HfSiON films was measured by single-wavelength (He-Ne: 633nm) ellipsometry at fixed reflective index of 2. Atomic concentrations in HfSiON were determined by XPS analysis. In order to evaluate the electrical properties of HfSiON, poly-Si gated MOSFETs were fabricated using conventional CMOS process. A quantum mechanical C-V simulator [7] was used for extraction of EOT.

3. Results and Discussions

***P**ost-**D**eposition **A**nnealing*

By applying N_2-PDA, $HfSiO/SiO_2$ was densified, resulting in reduction of optical thickness of the gate stack ($t_{HfSiO}+t_{SiO2}$). However, optical thickness increased due to lengthening the PDA period (Fig.2). According to the XPS analysis, as-deposited HfSiO contains excess oxygen (O/(Hf+Si)>2, Fig.3). The thickness increase is presumably due to the Si substrate oxidation by the excess oxygen. Even using the PDA period giving the minimum optical thickness, the leakage currents of post-deposition annealed samples are larger than that of sample without PDA (Fig.4).

***P**ost-**N**itridation **A**nnealing*

PNA also brings about reduction in the optical thickness of gate dielectrics (Fig.5), especially in N_2 at above 1000°C. Contrary to the case of PDA, PNA is effective for reducing the leakage current in EOT-Jg plot (Fig.6). Due to the interfacial layer thickness increase, additional oxygen in PNA ambient prevents realization of EOT of less than 1nm. PNA is also effective for improving electron mobility (Fig.7). Although there is a slight decrease in electron mobility by eliminating the oxygen in PNA ambient, 88% of that of SiO_2 is obtained even by N_2 PNA.

There are some concerns about the generation of oxygen defects in HfSiON by N_2 PNA. Since PBTI is believed to be due to the electron trapping by oxygen defect levels in HfSiON, PBT stress immunities were compared. It was confirmed that V_{th} shift due to the electron injection was sufficiently small and almost the same for the samples with applied N_2 and 0.1% O_2 PNA, respectively (Fig.8).

Sub-1nm HfSiON Gate Dielectrics

By using an ion mode plasma nitridation, interfacial layer growth can be further suppressed. Combining the optimized ion-mode plasma nitridation and N_2 PNA at 1050°C, EOT of 0.81nm with leakage current density of 0.74A/cm^2 at V_g of 0.7V was successfully achieved (Fig.9). To our knowledge, this is the smallest value reported so far for MOCVD based HfSiON gate dielectrics using poly-Si gate electrode. The electron mobility at 0.8MV/cm was 235cm^2/Vs (76% of SiO_2) (Fig.10). Because of low interface state density and small EOT, excellent S-factors of 64mV/dec. and 67mV/dec. for nMOS and pMOS, respectively, were obtained (Fig.11).

As V_{th} of pMOSFET is excessively high due to the Fermi-level pinning [8], introduction of metal gate electrodes with proper work function is necessary for LOP devices. Further scaling of EOT down to 0.75nm by decrease of pre-deposition IFL thickness can be realized (Fig.12). However, the excessive decrease brings about the increase of positive fixed charge density due to the interface nitridation (Fig.12).

4. Conclusions

It was shown that PNA without oxygen is indispensable to achieve sub-1nm EOT HfSiON with high mobility, whereas PDA is unnecessary. The fabrication of 0.81nm-EOT HfSiON gate dielectrics with gate leakage current of 0.74A/cm^2 at 0.7V and the electron mobility of 235cm^2/Vs at 0.8MV/cm (76% of SiO_2) has been demonstrated. HfSiON has the potential to meet the requirements of the gate dielectrics for LOP devices in hp45 and hp32 node.

Acknowledgements

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References

[1] S. Inumiya et al., VLSI Tech. Symposium, p.18, 2003.
[2] K. Sekine et al., Tech. Dig. IEDM, p.103, 2003.
[3] The International Technology Roadmap for Semiconductors 2004
[4] M. Hiratani et al., Jpn. J. Appl. Phys. Vol.41 p.4521, 2002.
[5] T. Aoyama et al., Mat. Res. Soc. Symp. Proc., vol.786, p.273, 2004.
[6] S. Inumiya et al., Ext. Abstr. (Spring Meet. 2005); JSAP, 30p-ZB-16.
[7] S. Saito et al., IEEE Electron Device Lett., Vol. 23, p.348, June 2002.
[8] C. Hobbs et al., VLSI Tech. Symposium, p.9, 2003.

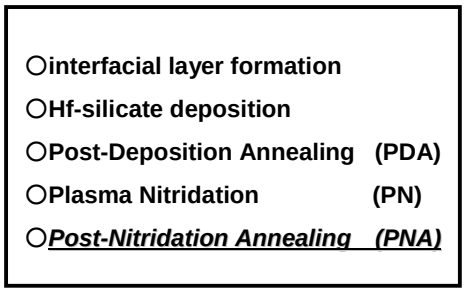

Fig. 1 Process flow of MOCVD based HfSiON gate dielectrics using plasma nitridation in this work.

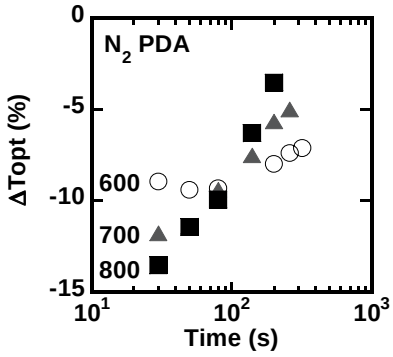

Fig. 2 Optical thickness change (from as-deposited thickness) dependence on N_2 annealing time at various temperatures.

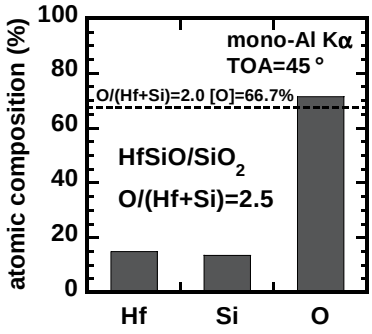

Fig. 3 Atomic compositions of Hf, Si and O in as-deposited $HfSiO/SiO_2$ stack structure, determined by XPS.

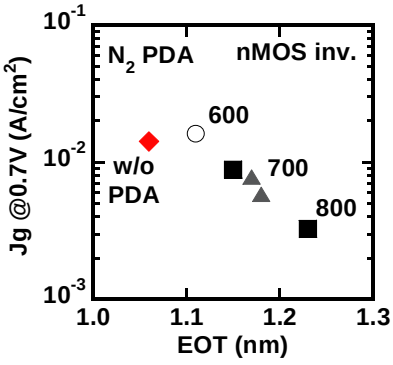

Fig. 4 EOT-Jg relationships for various PDA conditions. (80s at 600°C, 50s and 80s at 700°C, 30s and 80s at 800°C)

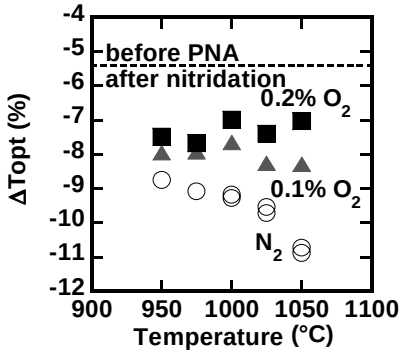

Fig. 5 Optical thickness change (from as-deposited thickness) dependence on PNA temperature for various ambients.

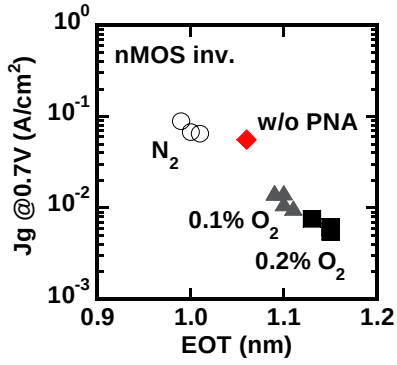

Fig. 6 EOT-Jg relationships for various PNA ambients. (1000 to 1050°C for N_2, 950 to 1050°C for 0.1%O_2 and 950 to 1000°C for 0.2% O_2)

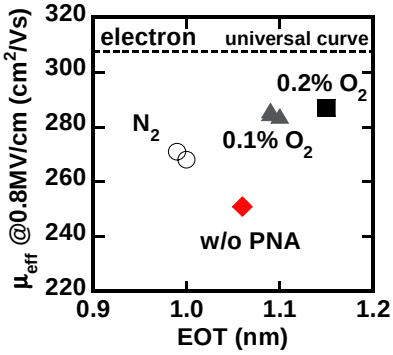

Fig. 7 Electron mobility dependence on EOT for various PNA ambients.

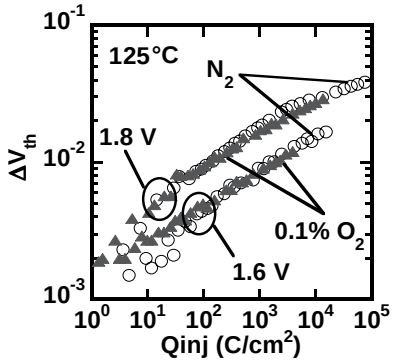

Fig. 8 V_{th} shifts dependence on injected charge density for PNA at 1050°C in N_2 or 0.1% O_2 ambient.

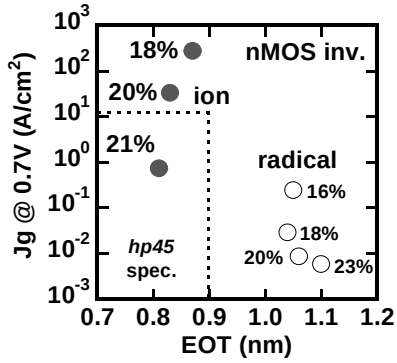

Fig. 9 EOT-Jg relationships of ultra-thin HfSiON films with PNA at 1050°C in N_2 for ion and radical mode nitridation.

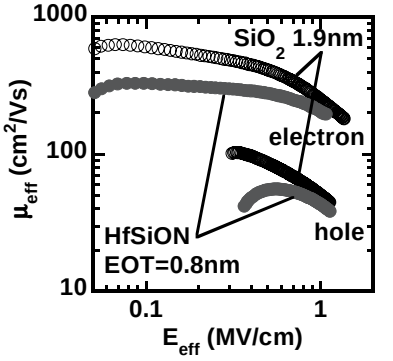

Fig. 10 Electron and hole effective mobility of ultra-thin HfSiON films and thermal oxide for effective electrical field.

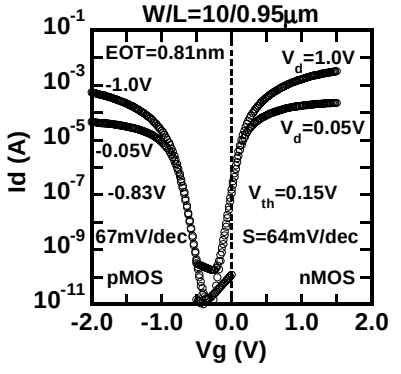

Fig. 11 Id-Vg characteristics of n+/p+ poly-Si gated MOSFETs with 0.81nm EOT HfSiON gate dielectrics.

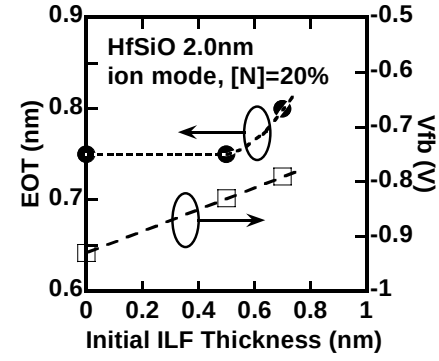

Fig. 12 EOT and V_{fb}(nMOS) dependence on pre-deposition IFL thickness. (HF-last = 0nm, SiO_2 0.5nm and SiO_2 0.7nm)

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