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NBTI Dependence on Dielectric Thickness in Ultra-scaled HfSiO Dielectric/ ALD-TiN Gate Stacks

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Abstract:

NBTI of the $HfSiO_x$/TiN gate stack is investigated as a function of the dielectric thickness. It is shown that as the thickness of the $HfSiO_x$ layer is reduced below 20Å, the NBTI mechanism approaches the mechanism that induces H-reaction diffusion. Conversely, for thicker $HfSiO_x$ dielectrics, a combination of H-reaction-diffusion and charge detrapping from the bulk $HfSiO_x$ contribute to NBTI.

1. Introduction

High-κ dielectrics, along with metal gate electrodes have been proposed to replace SiO_2 and poly-Si to continue gate stack scaling [1]. Although significant research has focused on high-κ dielectrics, such as hafnium oxide (HfO_2) and hafnium silicate ($HfSiO_x$), there is no general consensus on the reliability mechanisms of these materials under long-term electrical stress. Negative bias temperature instability (NBTI) has been empirically attributed to interface state generation resulting from hole injection in SiO_2/p+ poly-Si pFET gate stacks [2]. Recent NBTI research on high-κ dielectrics has shown that a similar mechanism also applies to high-κ gate stacks [3,4]. However, high-κ dielectrics have been shown to have significant "neutral" and charged trap centers, which can reversibly trap electrons and holes [5-7]. In this paper, NBTI characteristics of $HfSiO_x$ (30% SiO_2) with TiN gate electrode are investigated at various dielectric thicknesses to deconvolute the various mechanisms.

2. Sample Fabrication and Measurements

Figure 1 shows the CMOSFET processing flow used to fabricate the samples. On the HF-cleaned wafer, 10Å of interfacial oxide is grown, followed by atomic layer deposition (ALD) $HfSiO_x$ (30% SiO_2 – 18Å, 22Å, 26Å and 30Å) using $Hf[N(CH_3)C_2H_5]_4$ (TEMAHf) and $Si[N(CH_3)C_2H_5]_4$ (TEMASi) precursors with ozone oxidant (Post Deposition Anneal - 700C for 30s). The ALD TiN gate electrode is then deposited. The remaining transistor flow is standard and yielded wafers with excellent across-wafer-uniformity, EOT of 10-15 Å and electron mobility approaching universal channel mobility. Fig. 2 shows that Jg-EOT and μ-EOT are among the best reported for EOT ~10 Å. Fourier Transform Infrared Spectroscopy of the films shows an increase in the O-Si-O bond for thinner $HfSiO_x$ and a shift to the left (Fig. 3), indicating improvement in the quality of the SiO_2 interface. The NBTI tests are performed on 10×1 μm pMOS devices, with source, drain, and substrate grounded during the stress. The samples are stressed using a constant voltage for 1000s. The transconductance (gm) and threshold voltage (V_{TH}) are extracted using Id-Vg sweeps performed during periodic interruptions of the stress. Measurements are performed at various stress voltages and 3 different temperatures - Room Temperature (RT), 75°C and 125°C.

3. Results and Discussion

The threshold voltage shift in SiO_2 is believed to be due to the "hydrogen reaction-diffusion" (H° R-D) model. It has been shown mathematically that the threshold voltage shift follows a power law relationship with time with exponent n~0.25 [2]. The power law exponents are extracted from the slope of the log(ΔV_{TH}) vs log(time) plot. Fig. 4 and 5 show $\Delta(V_{TH})$ vs time for the thin $HfSiO_x$ (18Å), with various stress voltages and different temperatures. The power law exponent obtained for the thin $HfSiO_x$ is ~ 0.22-0.23. For the thick silicate however, the extracted power law exponent is ~0.14-0.16 (fig. 6 and fig. 7), indicating an additional component in the V_{TH} instability. Along with the threshold voltage shift we observe a downward shift in the peak transconductance (Fig. 8 - 18Å $HfSiO_x$), indicating creation of interface traps. The said results can be explained assuming that two mechanisms occur concurrently when high-κ gate stacks are stressed with negative bias: (a) Si-H bonds are broken by hole injection, as in the case of SiO_2 [3] and (b) existing negative charges in the high-κ layer are detrapped [5]. Both (a) and (b) processes result in negative threshold voltage shift. The contribution of (b) is minimal in SiO_2 and the exponent "n" obtained is entirely due to interface state generation. In high-κ dielectrics, however, a combination of these mechanisms is in effect. The dependence of "n" on the thickness of the dielectric (Fig. 9) shows that, as the thickness of the $HfSiO_x$ layer is reduced, the "n" increases towards 0.25 (SiO_2). This phenomenon implies that as the thickness decreases, H° R-D dominates over the charge detrapping mechanism. As the $HfSiO_x$ layer is made thicker, charge detrapping becomes the dominant mechanism. The value of "n" is smaller for the thick dielectric because a large portion of the charge detrapping is transient and occurs within ~ 100μs of stress and subsequent V_{TH} shift is slower, leading to a smaller value of "n". Fig. 10 shows gm,max degradation at 10sec stress plotted as a function of stress field for RT, 75°C and 125°C. The increase in the slope of the curve is much more severe for the thin $HfSiO_x$ (18Å) than for the thick $HfSiO_x$ (30Å). A concurrent increase in $\Delta(V_{TH})$ is also observed to be more severe in the thin $HfSiO_x$ (18Å) (Fig. 10). This theory is consistent with recent research by Houssa et al [9], who reported that the power law exponent "n" decreases with increase in "Hf" content in the film. The worse degradation of gm,max in thin $HfSiO_x$ (18Å), as compared to the thick $HfSiO_x$ (30Å) can be attributed to poorer quality interface in the thin $HfSiO_x$, as explained before.

3. Conclusions

NBTI is investigated for highly scaled $HfSiO_x$. From the dependence of power law exponent on dielectric thickness, it is concluded that the H-reaction diffusion model is the dominant mechanism for thin $HfSiO_x$ (18Å). Conversely, for thick $HfSiO_x$ (30Å), a combination of the H-reaction diffusion and charge detrapping from existing trap centers in the bulk contribute to NBTI.

References:
[1] International Technology Roadmap for Semiconductors (ITRS), 2004
[2] M.A Alam, IEDM Tech. Digest, Dec 2003, Pg. 14.4.1.
[3] Houssa *et al.*, VLSI Tech. Symp. Digest, June 2004, Pg. 212.
[4] S.Zafar, VSLI, 2004.
[5] Harris *et al.*, IRPS Proceedings, 2005, p. 80.
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[9] Houssa et al, APL Vol 86, April 2005.

HF cleaning
SiO_2 Interface (10Å)
ALD 30% $HfSiO_x$ (18Å, 22Å, 26Å and 30Å)
PDA (700ºC, 30sec)
TiN / Polysilicon 1500 Å deposition
Gate predoping
N LDD/halo
Nitride spacer
N SD (Source and Drain)
SD RTA (1000ºC, 5sec)
Metallization
Forming Gas anneal (480ºC, 30min)

Figure 1: CMOS Transistor flow

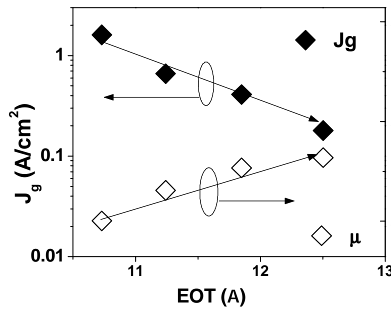


Figure 2: Jg vs EOT – EOT ~10.7Å w/ J_g ~1.6A/cm+2 and μ @ 1MV/cm ~87% Universal electron mobility

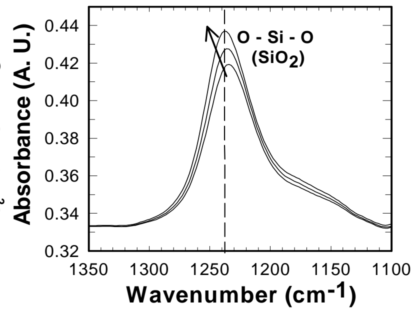


Figure 3: FTIR – shows increase in peak and shift to the left, indicating increase in O-Si-O bonds

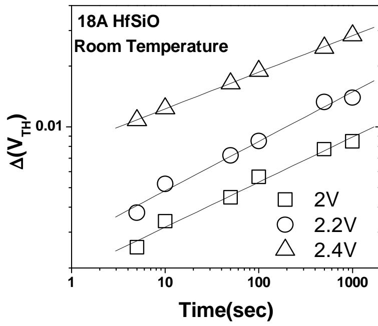


Figure 4: ΔV_{TH} as a function of time – 18Å HfSiO – Slope ~ 0.22-0.23 for different stress voltages

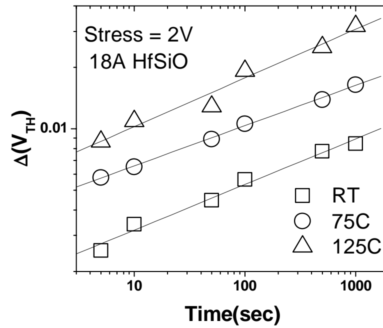


Figure 5: ΔV_{TH} as a function of time – 18Å HfSiO – RT, 75C and 125C show slope ~0.22-0.23

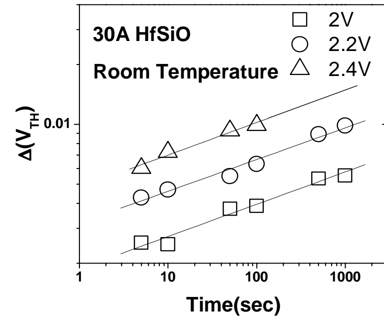


Figure 6: ΔV_{TH} as a function of time – 30Å HfSiO for different stress voltages show slope ~0.14-0.16

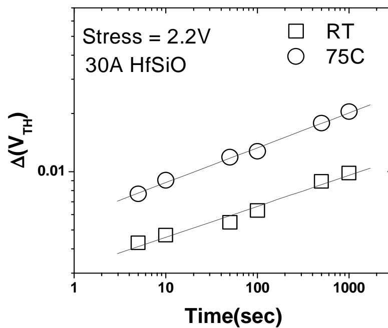


Figure 7: ΔV_{TH} as a function of time – 30Å HfSiO – RT, 75C and 125C show slope ~0.14-0.16

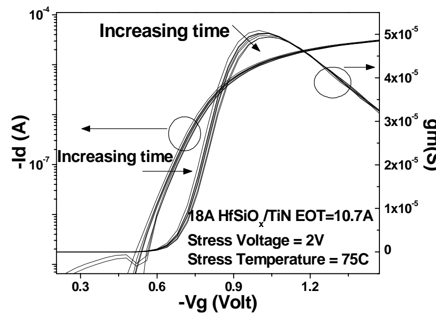


Figure 8: Id-Vg and gm-Vg – Show concurrent shift in both Vt and gm

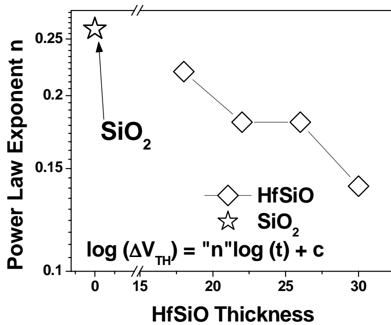


Figure 9: Power law exponent "n" increases as thickness of dielectric decreases

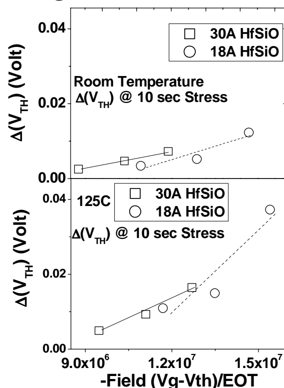
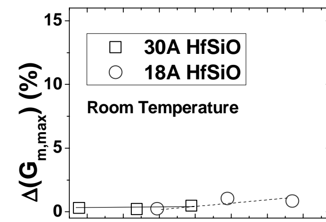
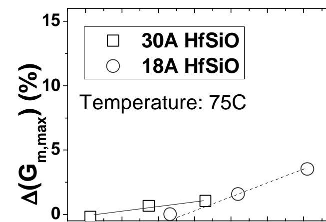


Figure 11: $\Delta(V_{TH})$ as a function of Field– Temperature dependence of slope is more severe for thinn $HfSiO_x$





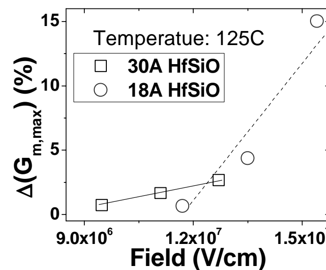


Figure 10: Gm, max degradation at 10 sec of stress – Temperature dependence of slope is more severe for thin oxide (dashed) than for thick oxide (solid)