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Effects of Nitrogen Concentration and Post-treatment on Reliability of HfSiON Gate Dielectrics in Inversion States

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Abstract

We have studied the effects of nitrogen concentration ([N]=N/(Hf+Si+O+N)) and post-nitridation anneal (PNA) conditions on reliability of MOSFET with HfSiON gate dielectrics in inversion states. Though they are almost independent in pMOS case, higher [N] and lower PNA temperature are effective for reducing SILC in nMOS. Since the increase of SILC in nMOS is caused by the crystallization in the HfSiON film, crystallization control is important for improvement of reliability in nMOS.

Introduction

TDDB reliability is one of the most serious problems for HfSiON gate dielectrics. Accumulation breakdown (BD) has been much reported, but there have been only a few studies on inversion [1-3]. However, reliability in inversion is more important than accumulation, because accumulated bias is not practically stressed. To obtain reliable CMOSFETs, further investigation of the inversion breakdown mechanism and exact prediction of lifetime in inversion states are required. In this paper, we will describe the effects of [N] and post-treatment on reliability of HfSiON gate dielectrics in inversion states.

Experimental

MOSFET fabrication flow is shown in Fig.1. Table I shows the [N] and PNA temperature of HfSiON (EOT=1.3nm). [N] were measured by XPS. PNA were carried out in diluted O_2 ambient. HfSiO deposition and post-deposition anneal (PDA) were performed at the same conditions among samples. TDDB measurements were carried out at 105°C with the area sizes of 100 μm^2. We applied monitor bias measurement method, which was gate leakage current (Ig) measurement at lower than stressed bias as shown in Fig.2, because it was sensitive to breakdown.

Result and Discussion

Fig.3 shows Ig-t characteristics in nMOS in inversion states (stress bias:2.6V, monitor bias:0.6V). The mechanism of BD is not clearly observed in the case of stress bias, but important information is revealed in the case of monitor bias. At primary stage, SILC increased gradually and then hard breakdown occurred. Higher [N] (sample (b)) is effective for reducing SILC. Moreover lower PNA temperature (sample (c)) contributes to that. HfSiON film is easy to crystallize with lower [N] conditions and higher PNA temperature condition [4]. Therefore, we investigated the relationship between SILC and crystallinity. From in-plane XRD spectra, diffraction peak attribute to HfO_2 crystal is observed in sample (a) ([N]=17%, PNA=1050°C). With the increase of [N] or with the decrease of PNA temperature, crystallization of HfSiON effectively suppressed (Fig.4). According to these results, we think that SILC is influenced by the crystallinity of HfSiON. Existence of grain boundaries causes the dangling bonds and electron traps [5] that may be responsible for SILC. Although in-plane XRD spectrum of sample (b) does not show the clear peak with crystalline, we speculate that there exist micro grains in the film. With lower PNA temperature, the existence of micro grain is suppressed. Therefore, it can be said that to prevent crystallization is effective for reducing SILC in nMOS. On the other hand, as indicated in Fig.5, Ig of pMOS never show such characteristics (stress bias:-3.2V, monitor bias:-1V). SILC are hardly shown among them. That means amount of traps which are responsible for SILC is almost independent of the crystallinity for pMOS. Fig.6 shows typical Qbd weibull distribution for nMOS and pMOS of sample (c). The 63%Qbd of pMOS is about one order of magnitude smaller than that of nMOS. Larger weibull β is obtained in pMOS (~1.4) in comparison with nMOS (~1.0). With the carrier separation measurement, we can see dominant carrier of Ig is electron in nMOS as shown in Fig.7. On the other hand, hole and electron are almost same at higher electric field in pMOS. Between nMOS and pMOS, amount of hole current, energy level of electron path and polarization are different (Fig.8). Since SILC is not shown in pMOS, it is thought that electron currents do not flow through the trap level. Torii *et al.* reported interfacial layer breakdown occurred with hole currents in pMOS [2]. As mentioned before, weibull β of pMOS is larger than nMOS, and SILC is independent of film condition. That means BD mechanism of pMOS is independent of film condition. Therefore, it is thought that interfacial layer BD due to hole current model may be suitable. In nMOS case, control of the film quality, especially crystallinity, is essential for reliability improvement in inversion state, but not so serious for pMOS reliability.

Conclusion

We have clarified that the effects of [N] and PNA temperatures are different between nMOS and pMOS for reliability of HfSiON gate dielectrics in inversion states. They are almost independent in pMOS case. In the case of nMOS, they strongly depend on the SILC at monitor bias. SILC have the relation with crystallinity in the film. Therefore, control of the crystallinity of HfSiON is effective for improving reliability in nMOS.

References

[1] Terai *et al. SSDM Tech. Digest* (2004) 74
[2] Torii *et al. IEDM Tech. Digest* (2004) 129
[3] Okada *et al. IEDM Tech. Digest* (2004) 721
[4] Sekine *et al. IEDM Tech Digest* (2003) 103
[5] Yamaguchi *et al. IRPS Proc.* (2003) 34

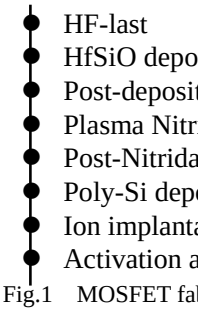

Fig.1 MOSFET fabrication flow.

Table I HfSiON nitridation conditions. Nitrogen concentration and post-nitridation anneal temperature were varied.

	(a)	(b)	(c)
[N]	17%	21%	21%
PNA temp.(°C)	1050	1050	1000

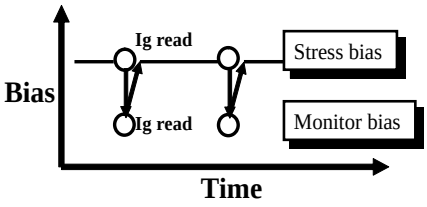

Fig.2 Measurement methods of gate leakage current at monitor bias.

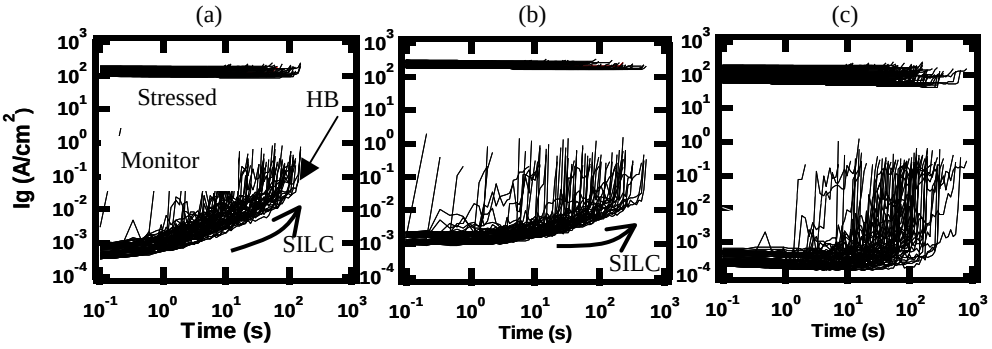

Fig.3 Ig-t characteristics of HfSiON gate dielectrics nMOSFET(EOT=1.3nm) in inversion states (stress bias:2.6V, monitor bias:0.6V). The sample conditions are listed in Table I.

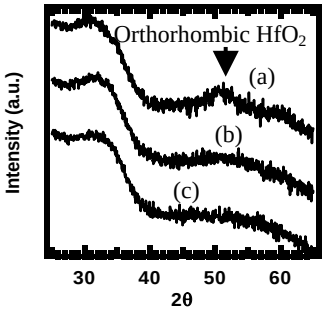

Fig.4 In-plane XRD spectra The sample conditions are listed in Table I.

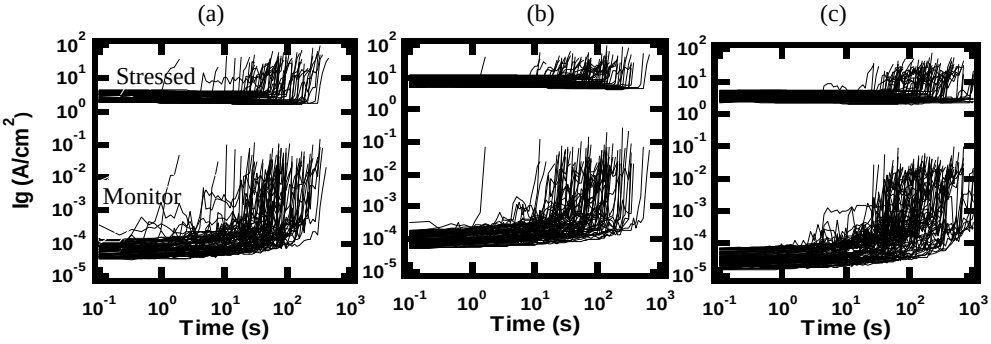

Fig.5 Ig-t characteristics of HfSiON gate dielectrics pMOSFET in inversion states. The samples are the same as Fig.2 (stress bias:-3.2V, monitor bias:-1V). The sample conditions are listed in Table I.

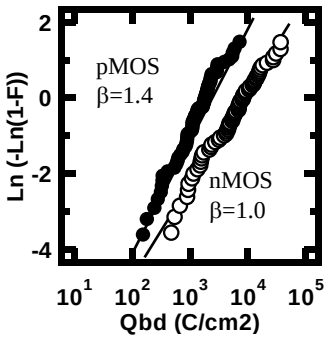

Fig.6 Qbd of nMOS and pMOS of sample (c); [N]=21%, PNA temp. = 1000°C.

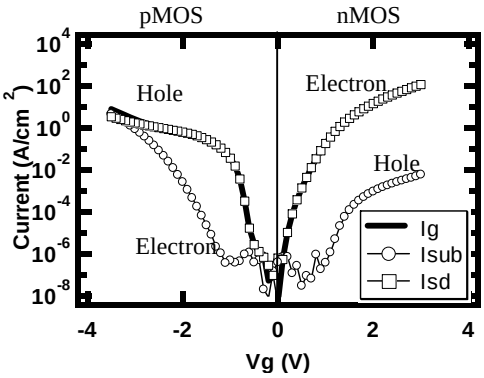

Fig.7 Carrier separation results of pMOS and nMOS in inversion states. Carrier types are shown below.
pMOS ; Isub=electron, Isd=hole.
nMOS ; Isub=hole, Isd=electron.

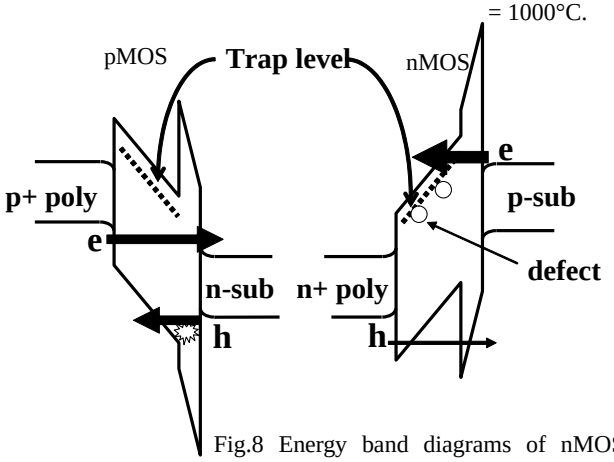

Fig.8 Energy band diagrams of nMOS and pMOS in inversion state. Electron trap level exist at near conduction band of HfSiON and it affect on the SILC in nMOS but not in pMOS.