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A novel inversion pulse measurement technique to investigate transient charging characteristics in high-k NMOS transistors

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Abstract

A novel inversion pulse measurement technique was developed to investigate the charging and relaxation behavior of high-k devices with μsec resolution. Our results indicate that V_{TH} instability can be significantly underestimated by conventional V_{TH} measurement technique. Also, it was found that charging and relaxation involve multiple processes including direct tunneling and thermally assisted charge redistribution.

Introduction

One of the challenges in the implementation of the high-k gate dielectrics is the stress-induced V_{TH} instability [1,2]. Peculiar feature of the V_{TH} instability in the high-k NMOS transistors is that it is reversible once the stress bias is removed [3,4]. Due to the transient nature of charging, the assessment of the V_{TH} instability is not straightforward and the interpretations of the results from different measurements have been controversial [5,6]. In part, these controversies arise from the insufficient time resolution of the conventional measurement techniques, which are generally required a relatively long time (msec to sec) to switch from the stress to sense regime and to perform V_{TH} measurements. As a result, the data collected with the conventional method are usually affected by the fast charge relaxation (de-trapping) processes in the μsec time range.

In this work, charge trapping and relaxation characteristics of TiN/Hf-silicate NMOS devices are characterized by a novel inversion pulse technique that enables the V_{TH} measurement with the μsec resolution.

Results and Discussion

The fabrication process and gate stack structure of the TiN/HfSiO NMOS devices used in this work are summarized in Table 1. Fig. 1 shows a typical V_{TH} shift and relaxation under the positive bias stress. Significant V_{TH} shift occurs at the beginning of a stress cycle and, as the stress continues, the V_{TH} increase rate is drastically reduced. Very limited subthreshold swing degradation during stress indicates that most of the V_{TH} shift can be attributed to charge trapping within the bulk of high-k dielectric [7]. Similar to charging, the relaxation of the V_{TH} shift shows saturation behavior after the rapid initial decrease. The fast relaxation raised questions on the validity of the conventional V_{TH} measurement during the stress, because time delay associated with the switching between the stress and Id-Vg measurement set-ups, as well as the time required for an Id-Vg measurement, can cause a significant measurement error leading to underestimation of the stress-induced V_{TH} shift [5,8].

To account for the effect of fast electron de-trapping, a new technique which can track V_{TH} relaxation in the μsec time scale has been proposed. The schematic diagram for the inversion pulse measurement technique is presented in Fig. 2 [9]. In this measurement, the base level of input pulse ($V_{in,1}$) is set to be slightly higher than V_{TH} to keep the device turned on during the stress and sense cycle.

Typical shapes of V_{in} and V_{out} pulses during the inversion pulse measurement are plotted in the Fig. 3. Fig. 4 explains the evolution of V_{out} during the stress cycle. Before the stress pulse has reached its peak value (at the Pre-stress stage), the drain current is described by Eq.(1). However, the charge trapping during the gate voltage ramp up and pulse peak period causes additional V_{TH} shift. Therefore, when the gate voltage goes back to its original $V_{in,1}$ value after the stress pulse (the Post-stress stage), the drain current decreases below its initial pre-stress level because of a reduced overdrive voltage ($Vg-V_{TH}-\Delta V_{TH}$). Accordingly, V_{out} increases by ΔV_{out} from the pre-stress V_{out} value, Eq.(2) in Fig. 4. From Eqs.(1) and (2), ΔV_{TH} can be obtained, Eq.(3) in Fig. 4. The derivation of Eq.(3) was simplified by assuming that the carrier mobility is not affected by a change of the surface potential resulted from a small charge trapping:

After the pulse stress, the V_{TH}, and subsequently V_{out}, values decrease gradually to their original values due to spontaneous electron de-trapping. Virtually flat dependence of V_{out} on the pulse width suggests that, in the gate stacks with small transient charging, most of the charging occurs during the pulse rising time (less than 5μs) and the effect of transient charging cannot be detected by the conventional pulse measurements with the longer rising times. Significant charging/relaxation of V_{TH} shift observed with the inversion pulse measurement technique indicates the superior sensitivity of this technique vs. others.

The time dependence of ΔV_{TH} after the various pulse stresses (ΔV_{TH} is calculated with Eq.(3) in Fig. 4 using the measured V_{out} time dependence at the post-stress) at room temperature are presented in Fig. 5(a) along with SiO_2 gate dielectric result for comparison. The data shows higher trapping and de-trapping behavior. The data are consistent with the previous report that a higher stress voltage results in both greater V_{TH} changes and higher relaxation rates [4]. The results clearly indicate that the stress-induced V_{TH} obtained by the conventional measurements, either DC or pulse, might be underestimated due to fast ΔV_{TH} relaxation during the switching time between the stress and Id-Vg measurement, as well as during the DC Id-Vg measurement. Indeed, the ΔV_{TH} values immediately after the stress and 250μsec after the stress demonstrate significant post-stress V_{TH} relaxation (Fig. 5(b)).

The dependence of the relaxation rate on both stress amplitude and duration is presented in Fig. 6. Under the given stress voltage, longer stresses seem to result in much lower electron de-trapping rates. Since the de-trapping process depends on the built-in potential caused by the trapped electrons, lower relaxation rate is indicative of more thermodynamically favorable redistribution of the trapped electron between the trap sites across the dielectric. Fast electron trapping shows weak temperature dependence in Fig. 7, reflecting primarily equilibrium thermal population of the traps filled in by direct electron tunneling from the substrate. On the contrary, relaxation rate significantly increases with temperature (Fig. 8), indicating that the de-trapping process is determined to a great degree by thermal activation, i.e. emission from the trap sites.

Charging during a long-term stress shows very strong temperature dependence (Fig. 9). This demonstrates that a long stress charging represents a complex process involving thermally-assisted re-distribution of the trapped charges and it can be suppressed at cryogenic temperature. It indicates that physical mechanism of long stress charging is a different process from the fast transient charging and the ΔV_{TH} change of high-k devices cannot be explained by the frequently used simple power law dependence on the stress time.

Summary

A novel “inversion pulse measurement technique” was developed and applied to investigate the charging and relaxation behaviors of high-k devices. It was found that the conventional measurement techniques might seriously underestimate the magnitude of charge trapping by ignoring the fast relaxation. It is shown that the relaxation behavior of fast transient charging is primarily determined by the thermal emission process. The temperature dependences of ΔV_{TH} suggest that different physical processes may contribute to the fast

transient and long stress charging phenomena. While fast trapping is mostly controlled by the direct electron tunneling, long stress charging is affected by temperature re-distribution of the trapped electrons.

References

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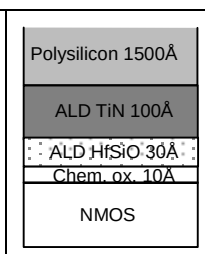
- o O_3 cleaning
- o ALD HfSiO deposition
- o PDA (700ºC, 1min in NH_3 ambient)
- o ALD TiN / Polysilicon deposition
- o Gate predoping
- o Nitride spacer (5nm)
- o N LDD/halo
- o Oxide spacer
- o N SD (Source and Drain)
- o SD RTA (1000ºC, 5sec)
- o Metallization
- o Forming Gas anneal (480ºC, 30min)



EOT : 14Å
V_{TH} : 0.71V

Table 1 Process flow and gate stack used in this experiment

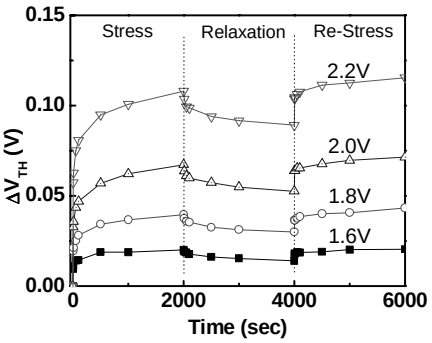


Fig. 1 Time dependence of V_{TH} values during stress with Vg= 1.6V to 2.2V and relaxation at Vg=0V

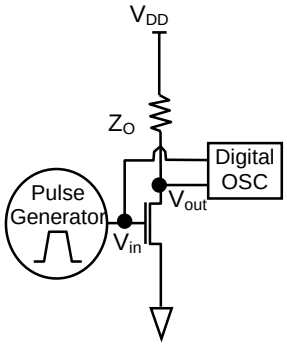


Fig. 2 Diagram of the inversion pulse measurement [9]

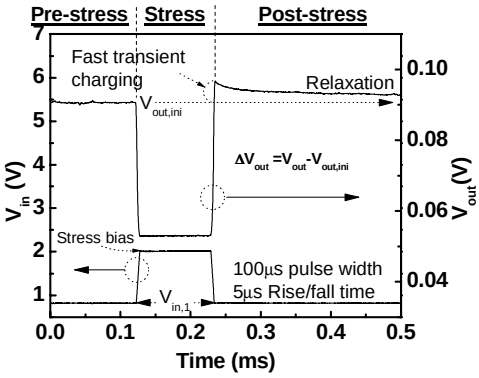


Fig. 3 Typical V_{in} and V_{out} signals of the inversion pulse measurement

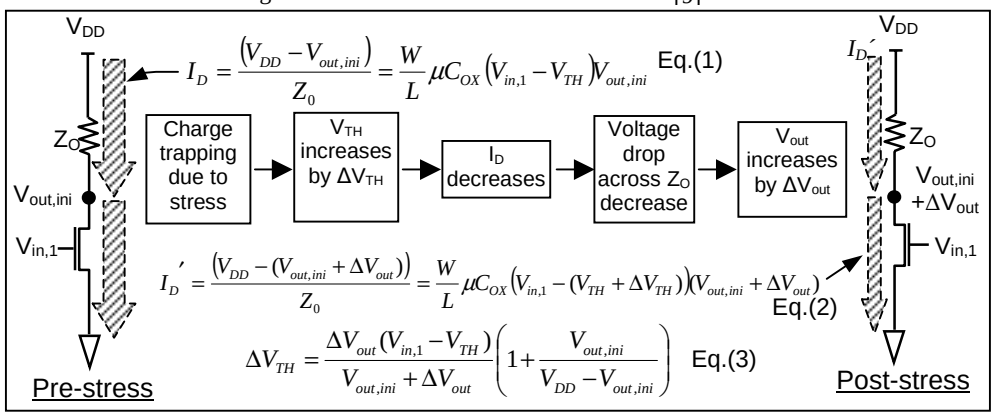


Fig. 4 Schematic for the V_{out} change during inversion pulse measurements and the calculation of the V_{TH} shift

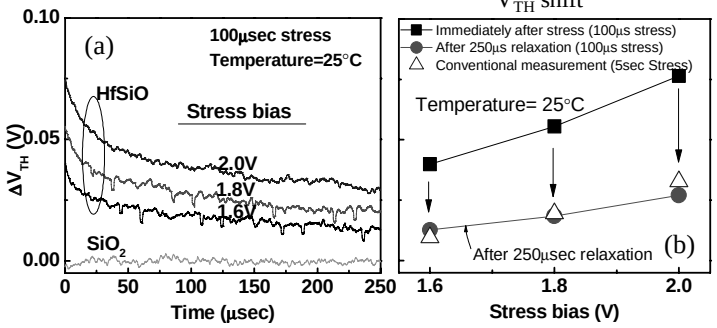


Fig. 5 (a) Post-stress time dependence of the V_{TH} shift induced by the 100μsec stress at Vg=1.6V, 1.8V and 2.0V (b) V_{TH} shift immediately after the 100μsec stress and after 250μsec post-stress relaxation period vs. stress voltage. Open symbols represent V_{TH} shift after 5sec stress measured using conventional Id-Vg method

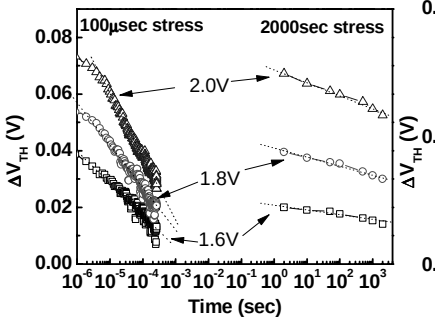


Fig. 6 Post-stress time dependence of V_{TH} shift induced by 100μsec and 2000sec stress at 1.6, 1.8 and 2.0V

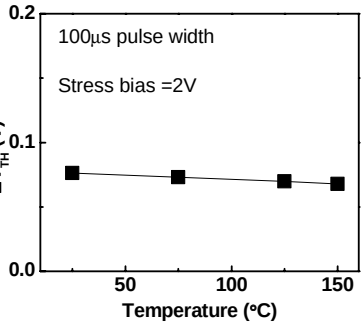


Fig. 7 Dependence of the stress-induced ΔV_{TH} on the stress temperature

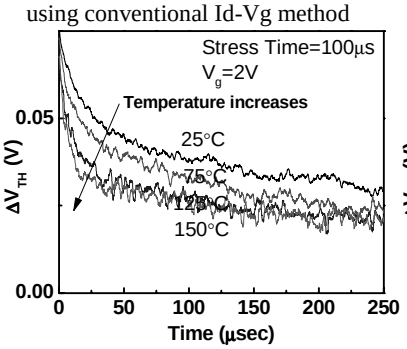


Fig. 8 Post-stress time dependence of the V_{TH} shift at different temperatures

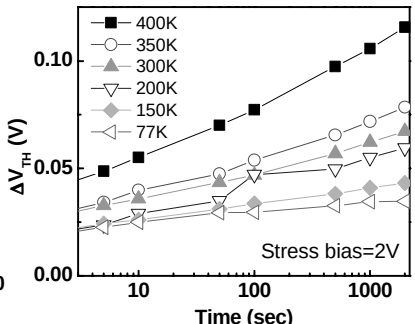


Fig. 9 Stress time dependence of the V_{TH} shift at different stress temperatures

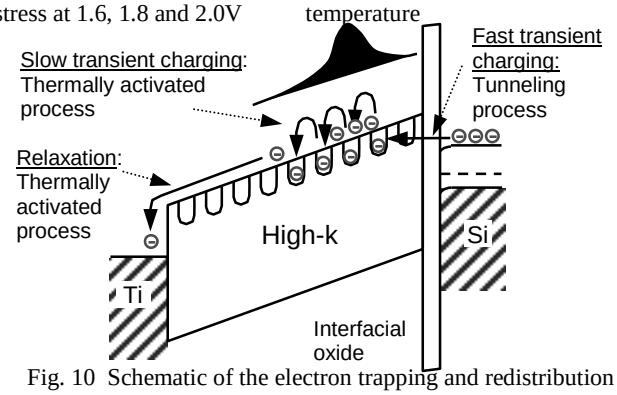


Fig. 10 Schematic of the electron trapping and redistribution processes. Fast transient charging is associated with the resonance electron tunneling into the traps. While the thermally activated charge redistribution process may contribute during long stresses