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# Evidence of Electrical and Structural Evolution of Gate Dielectric Breakdown Observed by Conductive Atomic Force Microscopy

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## 1. Introduction

Recently, it has been reported that structural deformations, such as dielectric breakdown-induced epitaxy at hard breakdown (HBD) as well as soft breakdown (SBD) spots of MOSFET, play an important role in breakdown event of gate oxide (Gox) [1,2]. On the other hand, the existence of net negative charges also has been reported after BD [3]. However, it remains unknown how these structural and electrical defects are generated and related to early degradation stages and how they evolve into BD events, due to the local and transient features of BD events and the difficulty of observation by conventional methods. Furthermore, accurate measurements are required to detect the minor electrical changes during degradation when using CAFM.

In this report, a new procedure is proposed in which pre- and post-BD stages on local spots are simulated by inducing high electric field and by monitoring the BD evolutions on Gox with accurate CAFM. Electrical and morphological degradations were observed prior to BD of Gox. Negative charges and structural hillocks were observed both pre- and post-BD, with similar lateral distributions much larger than injected contact area.

## 2. Experimental

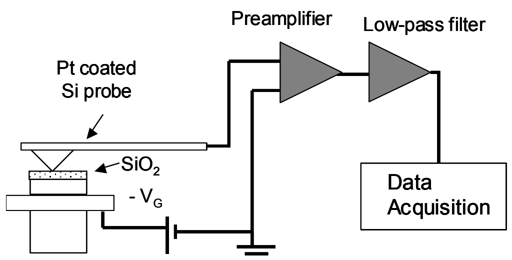


Fig. 1 Schamatics of CAFM. The conductive probe acts as a metal-gate electrode. Low-noise preamplifier is used for obtaining ultra-low current.

$SiO_2$ Gox of 5 nm on n-type Si substrate was used for measurement. A Schematic of the circuit of a commercially available CAFM is shown in Fig. 1, using Pt-coated Si probes as gate electrode, where bias is supplied by substrate voltage, which is defined as -$V_G$ here. Current–Voltage (*I-V*) measurements were carried out in vacuum (<1 x $10^{-5}$ Torr), where electrons were injected from n-type Si by FN tunneling into $SiO_2$ Gox, as shown in the inset of Fig. 2(a). A uniform FN tunneling current fits the simulation results well with accuracy of $\Delta I/I = \pm 33$ % down to 20 fA.

High-field FN stresses were applied to the Gox by a sequence of *I-V* ramps with fixed maximum $V_G$. The defect generations were investigated by comparison of sequential *I-V* characteristics with the fresh ones, whereas lateral damage distributions after *I-V* measurements were observed by simultaneous measurement of leakage current and topographical images at lower sensing voltages. Since the evaluation of a BD event strongly depends on the measurement procedure, it was performed carefully with the probe contacting the sample only during measurement to prevent discharge from the degraded spots.

## 3. Results and Discussions

Figure 2 shows (a) the *I-V* results of 5 sequential voltage ramps with a maximum $V_G$ of 8.8 V; (b) the subsequent current image at sensing $V_G$ = 7 V; and subsequent simultaneous images of (c) current and (d) topography at opposite polarity sensing $V_G$ = - 8 V; (e) topographic profile of (d). From Fig. 2(a), the 2$^{nd}$ *I-V* curve shows a positive shift $\Delta V \sim 0.5$ V against the fresh one, indicating electron trapping occurred during the 1$^{st}$ high field *I-V* ramp stress. But no obvious further shift was observed during the additional *I-V* stresses. From the current image in Fig. 2(b) at 7 V, the stressed area has a lower current shown as dark regions, compared to surrounding fresh locations, whereas the same area shows higher current as bright regions in Fig. 2(c) at opposite polarity sensing $V_G$ of - 8 V. A possible explanation is that negative charges were trapped at neutral traps during degradation by *I-V* stress, and the $\Delta$ V originated from the flat band shift due to buildup of negative charges in the Gox. Another phenomenon observed in Fig. 2(e) is the topographical change (~ 1.2 nm) of the measured hillock area against surrounding fresh areas in Fig. 2(d), which is found independent of measuring bias polarity, indicating a physical change occurred in addition to an electrical one. It is also found from Fig. 2(b)-(e) that the damaged area is ~ 8 × $10^3$ nm$^2$, larger than the contacted area of probe gate (~ 100 nm$^2$), indicating a lateral dispersion of the trap generation during *I-V* stress.

The BD event was often observed at sufficiently high field (~ 15 MV/cm), e.g. as shown in the inset of Fig. 3(a), which was a result of a single ramp of *I-V*. The consequent post-BD *I-V* ramp in very low voltage region was obtained as shown in Fig. 3(a). An almost ohmic *I-V* was observed with a shift of $V_G$ to the positive side as $\Delta$ V ~ 0.2 V, indicating the existence of negative charges. The subsequent current and topographical images with a sensing

$V_G = 0$ V were obtained as shown in Fig. 3(b) and (c); with the hillock profile as (d). Comparison of Fig. 3(b) and (c) reveals that the detrapping current has a lateral distribution corresponding to the edge of the hillock in (c), indicating local thinning location suffers BD first. In addition, the hillock in Fig. 3(d) is higher (~ 6.3 nm) than that in Fig. 2(e), whereas the lateral propagation of the BD spot is found to be of a size similar to that before BD, namely, ~ 100 nm in diameter, implying a progressive process of degradation and lateral propagation from pre-BD to BD.

The BD-evolution mechanism diagram is depicted in Fig. 4. It is considered that high current density induced local joule heating accompanied by thermal-electrical effects similar to electromigration deformed Si substrate toward the carrier injection direction even before BD. Furthermore, the Si deformation leads to more degradation of Gox by spreading defects laterally to a wider area, facilitating formation of percolation path to trigger a BD.

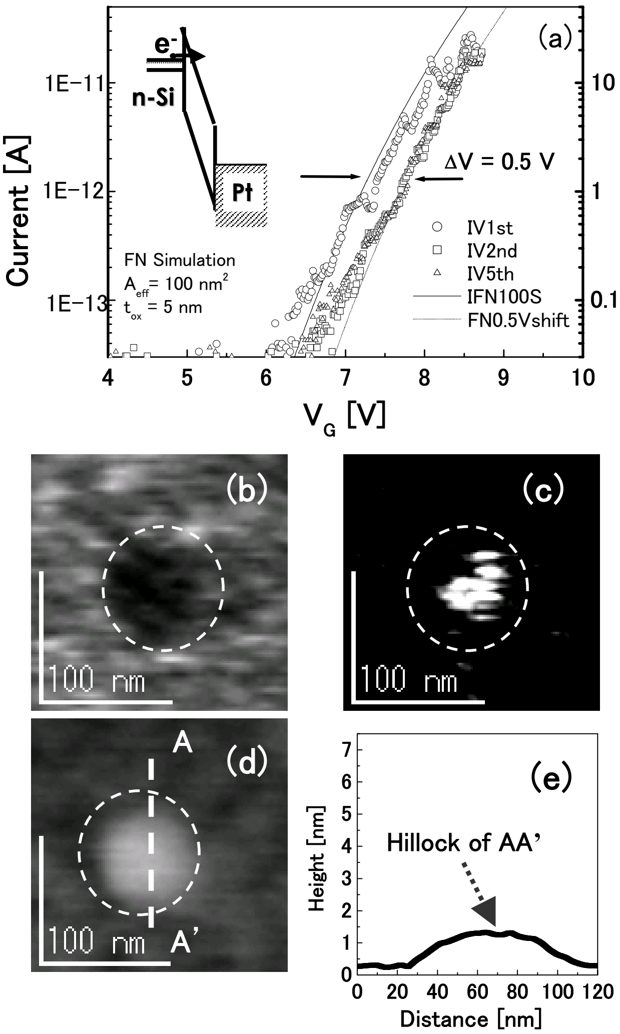


Fig. 2 (a) The *I-V* results of the 1st, 2nd and 5th ramps of 5 sequential *I-V* ramps. (b) The subsequent current image at $V_G = 7$ V; Subsequent simultaneous (c) current image and (d ) topographical image at $V_G = -8$ V; (e) Topographical profile of the hillock (~ 1.2 nm) along AA' in (d).

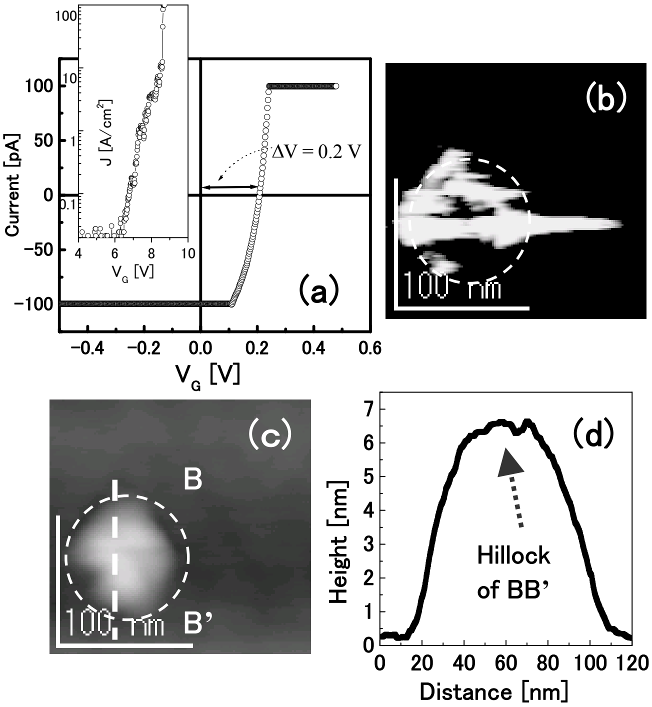


Fig. 3 BD during a single *I-V* ramp (inset). (a) Consequent post-BD *I-V* ramp immediately after BD at very low bias; Simultaneous (b) current and (c) topographical images at sensing voltage $V_G = 0$ V; (d) Topographical profile of the hillock (~ 6.3 nm) along BB' in (c).

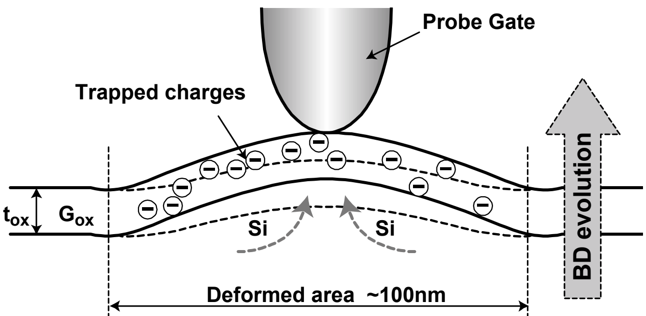


Fig. 4 The BD-evolution mechanism diagram. Si deformation occurs prior to and hastens the BD event. The topographical hillock grows with BD evolution.

## 4. Conclusions

Experimental evidence has been obtained that structural deformations accompanied by negative charge defects occurred prior to catastrophic BD in Gox. It is indicated that BD is a progressive process where thermal-electrical effects play an important role.


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## References


[1] K. L. Pey *et al., IEDM Tech. Dig.,* (2002) 166.

[2] C. H. Tung *et al.*, IEEE Electron Device Letts., **23** (2002) 526.

[3] T. Pompl *et al., IEEE 37th IRPS Proceedings*, (1999) 23.