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Thermal Degradation of HfSiON Dielectrics Caused by TiN Gate Electrodes and Its Impact on Electrical Properties

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1. Introduction

Metal gate electrodes on high-k dielectrics have gained considerable attention. Titanium nitride (TiN) is considered to be thermally stable and thus useful for p-type or mid-gap metal. However, as for TiN/HfSiON transistors, reduction of carrier mobility has been reported [1]. A possible explanation for this electrical degradation is reactions at the metal/high-k interface, but the details of the interface reaction and its impact on device performance are not yet fully understood. In this paper, we report on the physical and electrical characterizations of TiN/HfSiON gate stacks. We found that a crystalline TiO_2 layer is formed at the interface. Electrical degradation due to the thermal reaction was also investigated. Based on these results, we propose an interface reaction model, which determines the thermal budget of the metal/high-k gate stack.

2. Experimental

The HfSiON dielectrics were deposited by MOCVD [2]. Equivalent oxide thickness (EOT), measured using poly-Si electrodes, was 1.3 nm. The HfSiON film remained amorphous after activation annealing. The TiN electrodes were fabricated by PVD. The TiN/HfSiON/Si gate stacks were annealed in nitrogen ambient and then the TiN layers were selectively removed by wet etching. Residual Ti atoms on the etched surfaces were examined by TXRF. The crystallographic structure and surface morphology of the dielectric layer were investigated by reflection high-energy electron diffraction (RHEED) and AFM. Basic electrical properties were examined by C-V and I-V measurements.

3. Results and Discussion

Figure 1 shows residual Ti atoms detected by TXRF analysis after wet etching of the TiN overlayer. At low temperatures, the interface is stable and the TiN layer was thus completely removed by wet etching. However, after annealing at 700°C, interface reaction was found to form a Ti-containing layer that cannot be removed by H_2O_2 solution. The RHEED patterns shown in Fig. 2 revealed that a poly crystalline layer was formed at the TiN interface. The pattern analysis indicates that the poly crystalline layers were anatase or rutile-TiO_2 (Fig. 3). Figure 4 shows AFM images of the TiO_2 surfaces. The surface remains smooth at 700°C, but it becomes rougher at higher temperature. These results suggest that the TiO_2 layer degrades and further reaction with the gate dielectric occurs over 900°C. The reduction of the TXRF signal in this temperature range is thus probably due to further metal diffusion through the gate oxide or degradation of the TiO_2 layer against wet etching.

Figure 5 shows typical C-V and I-V curves of the TiN/HfSiON/Si capacitors before and after annealing. The changes in EOT and leakage current (I_g) are summarized in Fig. 6. Although the reaction at TiN/HfSiON forms the interface TiO_2 layer, there is no severe degradation in EOT - I_g characteristics up to 900°C. It is notable that the EOT slightly decreases at 700°C owing to the formation of the TiO_2 layer with higher permittivity. However, high -temperature annealing at 1100°C results in interface oxide growth and dielectric degradation of the high-k layer. Figure 7 shows changes in the V_{fb} and conductance estimated from Fig. 5. Note that the thermal reaction that causes a shift in V_{fb} and an increase in D_{it} occurs at 900°C.

Figure 8 illustrates a reaction model at the TiN/HfSiON interface. The gate stack is stable up to 500°C. Interface reaction forms the ultrathin TiO_2 dielectric layer at 700°C, but there is no severe degradation of electrical properties. After annealing at 900°C, we observed both V_{fb} shift and increased D_{it}, which are probably due to metal diffusion through the gate oxide. Moreover, further annealing causes dielectric degradation of the HfSiON and TiO_2 layers as well as oxide growth at the bottom interface.

4. Conclusions

We investigated reactions at TiN/HfSiON/Si interfaces and found that an ultrathin TiO_2 layer is formed at low temperature. The formation of the interlayer itself does not affect device performance drastically, but degradation of interface properties, such as V_{th} shift and increased D_{it}, occurs at 900°C. These findings indicate that detailed physical and electrical studies are indispensable for material selection and that improvement of the electrode quality and rapid thermal process is required to realize metal/high-k gate stacks.

Acknowledgements

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References

[1] K. Takahashi et al., Jpn. J. Appl. Phys. **44**, 2210 (2005).
[2] T. Aoyama et al., Extended Abstracts of IWGI 2003, p. 174.

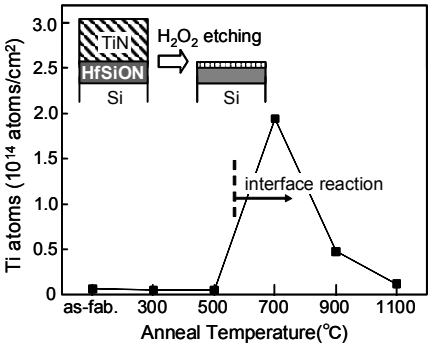


Fig. 1. TXRF analysis of residual Ti atoms.

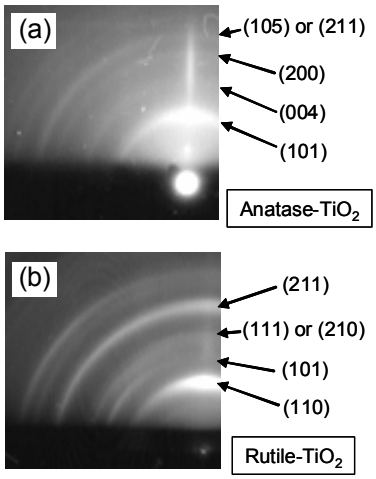


Fig. 3. RHEED pattern analysis after annealing at (a) 700 and (b) 1100°C.

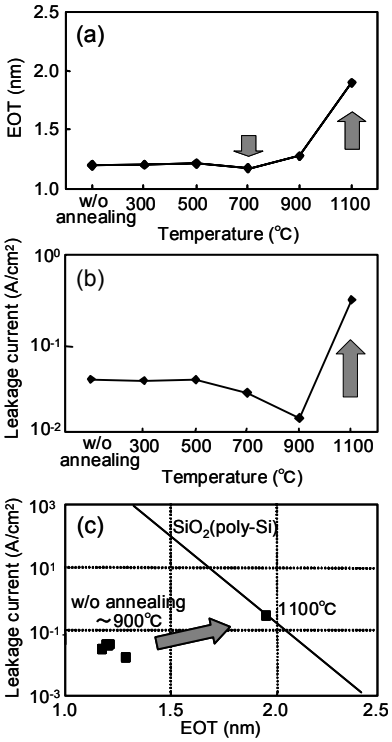


Fig. 6. Changes in EOT and I_g caused by annealing; (a) EOT, (b) I_g, and (c) EOT vs I_g.

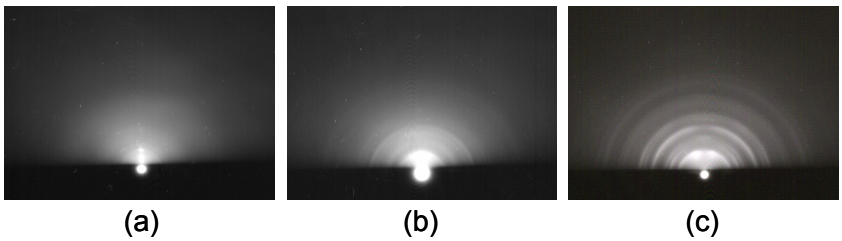


Fig. 2. RHEED patterns obtained from the TiN/HfSiON interface after annealing at various temperatures for 30 seconds; (a) 500°C, (b) 700°C, and (c) 1100°C.

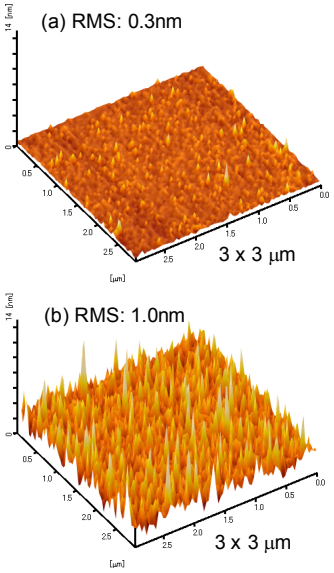
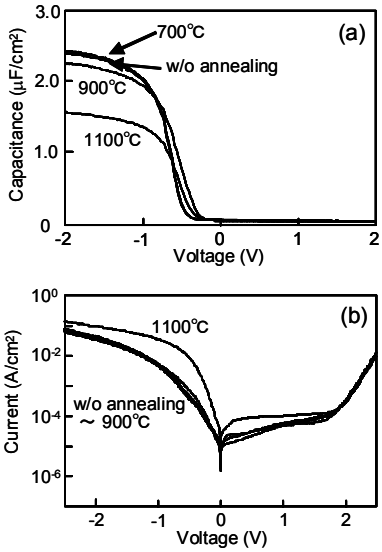


Fig. 4. AFM images obtained after removing TiN by wet etching; annealing was performed at (a) 700 and (b) 900°C.



5. Typical (a) C-V and (b) I-V characteristics of TiN/HfSiON/Si capacitors.

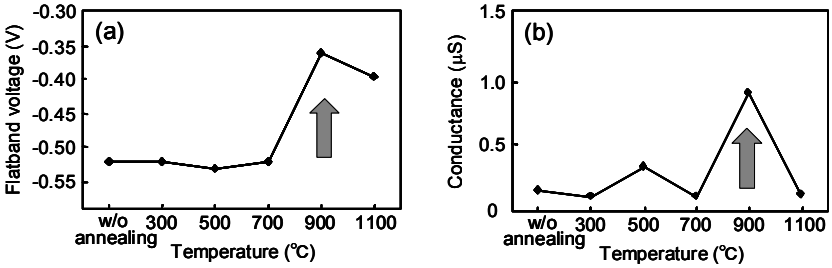


Fig. 7. Changes in (a) V_{fb} and (b) conductance due to annealing.

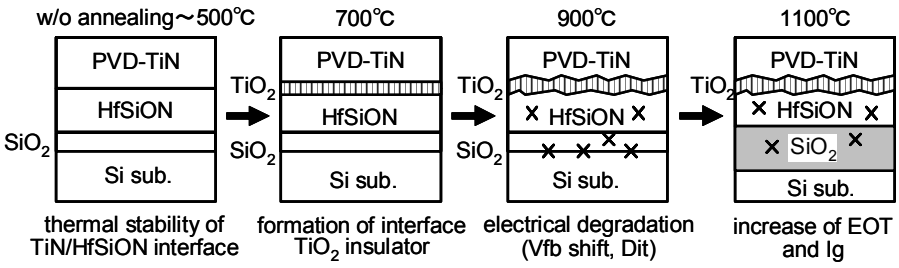


Fig. 8. Schematic illustration of interface reaction at TiN/HfSiON gate stack.