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Reliable Extractions of EOT and V_{fb} in Poly-Si Gate High-k MISFETs through Advanced Modeling of Gate and Substrate Capacitances

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1. Introduction

Equivalent oxide thickness (EOT) and flatband voltage (V_{fb}) are basic and important parameters in MIS devices. For their extractions, it is necessary to consider both the gate interface capacitance (C_{poly}) and the substrate surface capacitance (C_{sub}) accurately. On one hand, however, most reports on poly-Si gate high-k MISFETs do not care about the defect charges in high-k dielectrics, giving erroneous EOT [1]. On the other hand, no systematic, experimental examinations are reported on the effect of Si surface quantization at flatband [2]. In this paper we discuss both of these issues, and attain reliable extractions of EOT and V_{fb} through an accurate model of C_{poly} and C_{sub}.

2. Experimental

High-k MISFETs with n^+poly-Si/$HfAlO_x$/SiO_2/p-Si structures and n_{sub}=1x$10^{16}$$cm^{-3}$ were fabricated. MOS capacitors with n^+poly-Si/SiO_2(4.5nm)/p-Si were also fabricated on the substrates of n_{sub}=10^{16}, 10^{17}, $10^{18}$$cm^{-3}$. C-V characteristics were measured on these devices.

3. Results and Discussion

Figures 1 and **2** show the basic concept of this work. The characteristic lengths λ_{poly} and λ_{sub} corresponding to C_{poly} and C_{sub} were described as the double layers consisting of a quantization layer (λ_{qd} in poly-Si or λ_{qd}^{sub} in Si-substrate) and a free carrier layer (λ_s or λ_s^{sub}), respectively.

(a) C_{poly} in the presence of high-k dielectric defect charges

Large density of defect charges in high-k dielectric and its interfaces causes a relative shift of the electric field strength in the Si-substrate and poly-Si gate (Fig. 1). Exact extraction of EOT requires the consideration of this shift, because C_{poly} can become comparable to C_{sub} due to this effect. The quantization layer in poly-Si, λ_{qd}, and the electric field E_s at the boundary between λ_{qd} and λ_s, can be solved with the coupled equations:

$$\varepsilon_{Si}E_s = qn_{poly}\lambda_{qd} + q\,(N_{acc}+N_{ox}), \quad (1)$$

$$\lambda_{qd} = (h^2/4\pi^2 m^* qE_s)^{1/3}. \quad (2)$$

The free carrier layer thickness λ_s can then be derived from E_s with an analytical expression. **Figure 3** shows λ_{poly}=λ_{qd}+λ_s as a function of the substrate charge density N_{acc} in the case of N_{ox}=0. This C_{poly} model agrees well with the quantum mechanical simulation in Ref.[2], except for the inclusion of screening length adjacent to the depletion layer. As shown in **Fig. 4**, the defect charge N_{ox} causes a shift of the λ_{poly}-N_{acc} curve along the horizontal axis, relative to N_{ox}=0. This C_{poly} model was confirmed to be accurate in EOT extraction of SiO_2 MOS devices with N_{ox}=0. It was then applied to the C-V curve of an n^+poly-Si/$HfAlO_x$/SiO_2/Si MISFET (**Fig. 5**). With a proper fitting procedure, we obtained the parameters for the λ_{poly} model as N_{ox}=8x$10^{12}$$cm^{-2}$ and n_{poly} = 4.7x$10^{19}$$cm^{-3}$. The quantity ($\varepsilon_{Si}/C$-$\lambda_{sub}$-$\lambda_{poly}$) becomes a constant over a wide range of N_{acc}, indicating a reliable EOT extraction.

(b) C_{sub} at flatband condition for highly doped Si surface

The common definition for the flatband condition is C_{sub}=$\varepsilon_{Si}/\lambda_{Debye}$, where λ_{Debye} is the Debye length. For a highly doped Si-substrate, this definition gives an incorrect V_{fb} that significantly deviates from the gate-substrate work function difference as shown in **Fig. 6**. Inclusion of the Si-substrate quantization at flatband via λ_{qd}^{sub}= $(h/2\pi)/(2m^*k_BT)^{0.5}$ [2] gives a better result, while an opposite deviation from the work function difference curve still remains at high N_{sub}.

To study the cause of this deviation, we performed a new V_{fb} extraction focusing on the free carrier layer. For SiO_2 MOS capacitors with a high n_{poly}, $d(1/C^2)/dV_g$ is given by:

$$d(1/C^2)/dV_g = (2/\varepsilon_{Si})\Sigma_i\, d\lambda_i/dQ = (2/\varepsilon_{Si})d\lambda_s^{sub}/dQ. \quad (3)$$

This is because λ_{poly} and λ_{qd}^{sub} near the flatband condition have negligible dependence on substrate surface charge, Q. As shown in **Fig. 7**, detailed calculation of $d\lambda_s^{sub}/dQ$ leads to the result that V_{fb} can be extracted from the value of $d(1/C^2)/dV_g$ with the ratio of **Fig. 8** relative to $d(1/C^2)/dV_g$ in the depletion region. Note that we have derived the ratio for two kinds of flatband conditions, which originate from different terminations of the ionized dopant charge in the quantization layer (**Fig. 9**). **Figure 10** summarizes the extracted V_{fb} as a function of N_{sub}. The "flat substrate" condition shows a deviation of V_{fb} in high N_{sub}, while the "flat dielectric" condition gives negligible deviation from the work function difference. The deviation of the former is quantitatively explainable by the potential drop across the gate dielectric (4.5nm SiO_2). Thus, the correction is necessary for the inevitably existing charge in the quantization layer. The V_{fb} at "flat dielectric" condition becomes a better reference to evaluate high-k dielectrics and the work function of the gate electrode.

4. Conclusions

It was demonstrated that reliable EOT extraction in high-k MISFETs is achieved by a C_{poly} model in which the electric field shift due to the defect charges in high-k dielectrics is taken into account. The substrate surface quantization at flatband must be considered for accurate V_{fb} extraction in MISFETs with highly doped Si-substrates. Care is needed for the V_{fb} shift due to the ionized dopant charge in the quantization layer.

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References: [1] K. Ahmed et al., *Ext. Abs. SSDM* p.218 (2004). [2] A. Spinelli et al., IEEE Trans. ED 47, 2366 (2000).

Present affiliation: a) Toshiba Corp. b) Seiko Epson Corp.

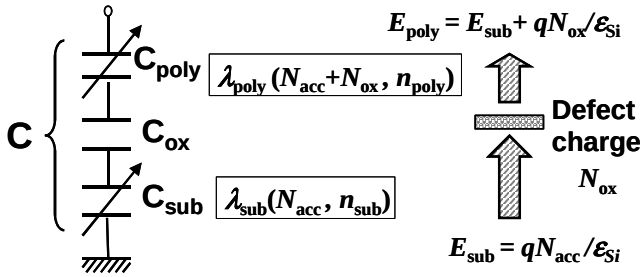

Fig. 1 Equivalent circuit for poly-Si gate MOS structures. Defect charges in high-k dielectric and its interfaces modulate the electric field from Si-substrate.

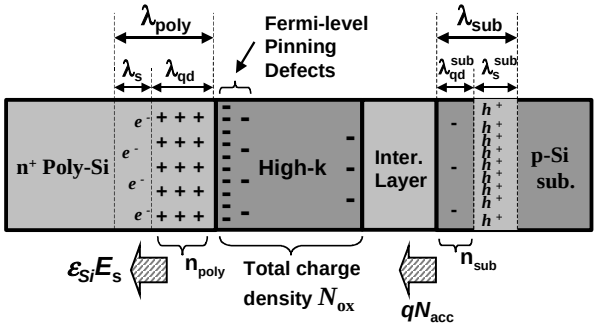

Fig. 2 Schematic diagram for interface capacitances. The poly-Si gate capacitance is composed of quantization layer λ_{qd} (an ionized dopant layer), and a free carrier layer λ_s. Similar model is also applicable to Si-substrate surface capacitance.

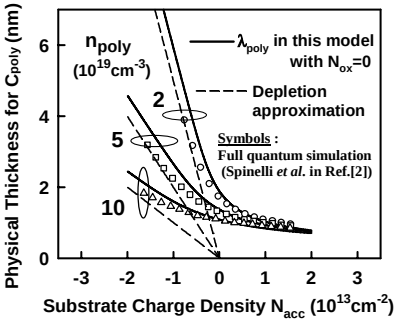

Fig. 3 Physical Thickness for C_{poly} (i.e. $\lambda_{poly}=\lambda_{qd}+\lambda_s$) for N_{ox}=0 in the present model as a function of N_{acc}. Comparison with the simulation results in Ref.[2] is also indicated.

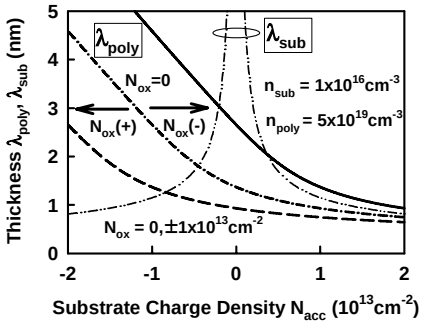

Fig. 4 Thickness for poly-Si gate capacitance λ_{poly}, as a function of N_{acc}, with defect charge density N_{ox} as a parameter. λ_{sub} is shown for reference.

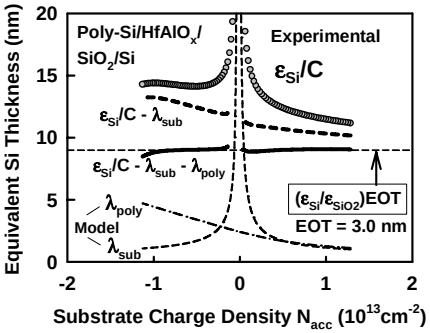

Fig. 5 Equivalent thicknesses in Si as a function of N_{acc}, where λ_{poly} is determined for N_{ox} =$8x10^{12}cm^{-2}$ and n_{poly} =$4.7x10^{19}cm^{-3}$.

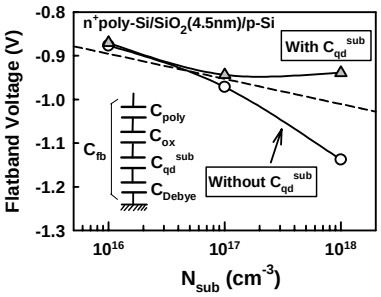

Fig. 6 V_{fb}'s extracted from C-V curves of SiO_2 MOS capacitors, with the incorporation of C_{qd}^{sub} as a parameter. Dashed line shows the work function difference between n^+poly-Si and p-Si.

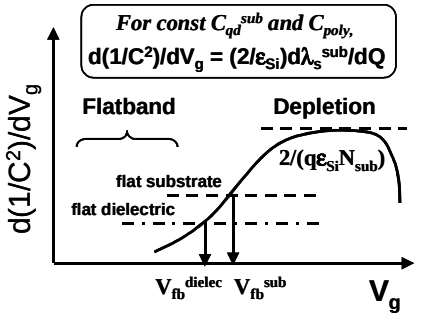

Fig. 7 Principle of V_{fb} extraction using the properties of a substrate free carrier layer. This method is valid when the electric field dependences of C_{qd}^{sub} and C_{poly} are negligible.

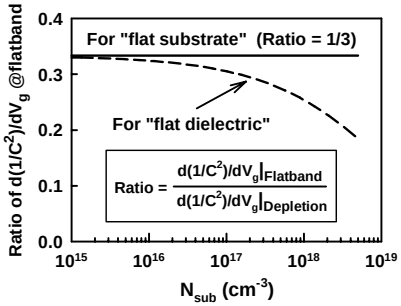

Fig. 8 The ratio of $d(1/C^2)/dV_g$ at flatband conditions relative to the depletion region. Two kinds of flatband conditions (see Fig. 9) were considered.

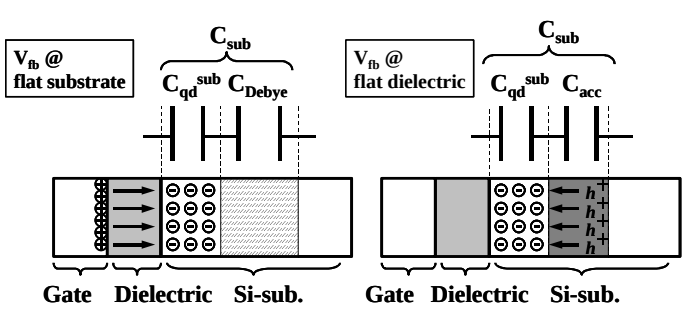

Fig. 9 Two kinds of flatband conditions due to different terminations of the ionized dopant charge in the Si-substrate quantization layer.

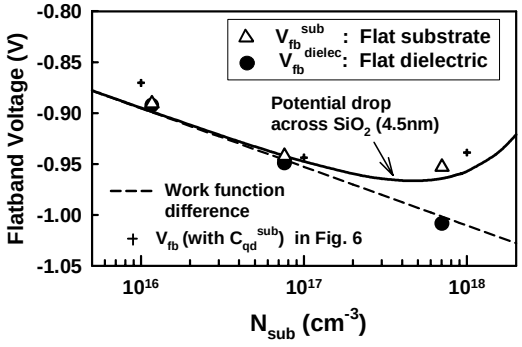

Fig. 10 V_{fb} from the new extraction method. Solid curve is a calculated V_{fb} for the "flat substrate" condition for MOS capacitors with 4.5nm SiO_2.