Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.844-845

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Material Characterization of Metal-germanide Gate Electrodes Formed by FUGE (Fully Germanided) Process

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1. Introduction

Fully silicided gate (FUSI) technology is the prime candidate for dual metal gate due to its compatibility with conventional CMOSFET fabrication process [1]. On the other hand, silicides with band edge work functions are necessary to control threshold voltage for bulk CMOS devices. As for PMOS, platinum silicide reveals the highest effective work function (Φ_{eff}) (~ 4.9 eV) [2], which is slightly small to achieve low V_{th}. Recently, fully NiGe gate has been reported as a new PMOS gate candidate with Φ_{eff} corresponding to valence-band edge (*Ev*) [3]. In order to develop bulk CMOS devices with fully germanided gate (FUGE), however, material characterization has not been sufficient yet, such as the work function values for alternative metal germanides and the thermal stability through the conventional back-end processing.

In this paper, Φ_{eff} values for metal (Pt, Ni, Ta, Er) germanides prepared by FUGE process were systematically investigated for the first time. We found these germanides reveal work function values covering NMOS, midgap and PMOS gates on SiO_2. $NiGe_x$ MIS stack is fully sustainable up to 600°C, if $NiGe_x$ is capped with a tungsten film. FUGE electrodes are successfully compatible with the HfSiON gate dielectric. It is found that Fermi level pinning (FLP) phenomenon, which limit the applicability of FUSI technology to Hf-based dielectrics [2], can also affect Φ_{eff} values at FUGE/HfSiON.

2. Experimental

Germanide gated MIS capacitors were fabricated on p-type Si(100) substrate with FUGE process, which is similar to FUSI process (Fig. 1). Ge and metal (Pt, Ni, Ta, Er) layers were sputtered consecutively on thermally grown SiO_2 or HfSiON/SiO_2. Then, the specimens were annealed at 400-800°C for 60 s in N_2 atmosphere to form germanide gates. C-V characteristics were measured after forming gas anneal at 400°C for 30 min. In some samples, tungsten layers were sputtered subsequently after metal formation.

3. Results and Discussion

A. Φ_{eff} value of germanide on SiO_2

Fig. 2 shows that the flat-band voltages (V_{fb}) of germanide gate MOS capacitors change depending on the constituting metal elements. The maximum difference of V_{fb} is 1.2 V, and the Φ_{eff} modulation range covers the energy of Si bandgap, corresponding to conduction-band edge (*Ec*) ($ErGe_x$: 4.05 eV) and *Ev* (Pt_3Ge_2: 5.19 eV) as well as that closed to Si-midgap ($TaGe_2$: 4.70 eV) (Fig. 3). The realization of Φ_{eff} value corresponding to *Ev* with FUSI is quite difficult, because the Φ_{eff} value of PtSi is 4.9 eV, which contains the highest vacuum work function (Φ_{vac}) metal (Fig. 4). The Φ_{eff} values of germanides are about 0.3 eV higher than those of silicides, realizing high Φ_{eff} values near *Ev* (Ni and Pt germanides).

It is well known empirically that Φ_{vac} values of pure metals are linearly related to Pauling's electronegativity (χ_M), $\Phi_{vac}= 2.27\chi_M+0.34$ [4]. The Φ_{eff} and χ_M for germanides and silicides are related in the same way as Φ_{vac} and χ_M for pure metals, under the assumption that the χ_M is a geometric mean of metal and Ge or Si (Fig. 5). This result shows the Φ_{eff} values of germanides and silicides are strongly influenced by electron binding energies of elements. We conclude that larger electronegativity of Ge than Si results in higher Φ_{eff} values of germanides than silicides.

B. Thermal stability of germanide for PMOSFET and W-cap layer effect

We also investigated the thermal stability of germanide gate electrodes with Φ_{eff} values for low V_{th} PMOS. The thermal stability through back-end processing, comparable to NiSi thermal stability, is needed for "gate last" FUGE process. A significant increase in gate leakage current was observed in the case of $NiGe_x$ gate electrode after 500°C annealing, presumably owing to the lower melting point of germanide than silicide (Fig. 6). On the other hand, $PtGe_y$ gate electrode has sufficient thermal stability; low leakage current was maintained until after 600°C annealing. W-cap layer effectively suppresses the increase in gate leakage current after 600°C annealing of $NiGe_x$ gate electrode, indicating that W/$NiGe_x$ is also a candidate gate structure. W-cap layer also inhabits $PtGe_y$ penetration into SiO_2 (Fig. 7), which is the cause of increase in gate leakage current after 800°C annealing.

C. Applicability of Germanide/HfSiON gate stacked structure

Fig. 8 shows that W-capped Ni and Pt germanides on HfSiON maintain low gate leakage current and stable Φ_{eff} values even after 800°C annealing, indicating superior compatibility to the cases on SiO_2. The Φ_{eff} values of germanides on HfSiON decrease to Si-midgap compared to those on SiO_2, which is similar to the silicide cases (Fig. 9). This result indicates that FLP occurs at germanide/HfSiON interfaces in the same manner as at silicide/HfSiON. However, Φ_{eff} values corresponding to near *Ev* (>4.9 eV) are still achieved at $NiGe_x$ and $PtGe_y$/HfSiON interfaces, in contrast to midgap Φ_{eff} value of PtSi/HfSiON system (Fig. 9). Therefore, germanide gate has a potential ability for low V_{th} PMOS with HfSiON gate dielectric.

4. Conclusions

We have investigated Φ_{eff} values and thermal stabilities of germanide gate electrodes formed by FUGE process. It is found that Φ_{eff} values of germanides cover the energy of Si bandgap, and are higher than those of silicides. The Φ_{eff} values corresponding to *Ev*, desired for low V_{th} PMOS, were realized even on HfSiON. In addition, W-cap layer effectively improves thermal stability of germanides and

makes Ni germanide gate electrode sufficiently stable for the back-end processing. In conclusion, Ni and Pt germanides are promising for PMOS "gate last" metal gate electrode.

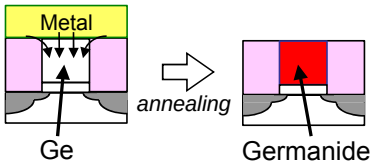

Fig. 1: Schematic of the FUGE (fully germanided gate) process. Germanide gate can be formed by solid-state reaction of Ge and metal.

5. Acknowledgment

We would like to express sincere thanks to Mr. K. Nakajima, and Mr. M. Sato for their valuable discussion and cooperation.

References

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[4] W. Gordy *et al.*, Phys. Rev. **24**, (1956) 439.
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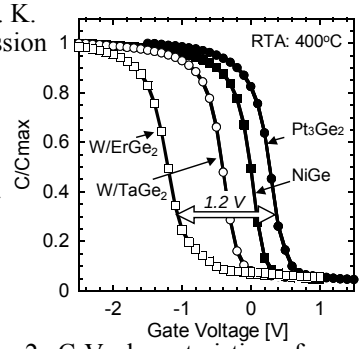

Fig. 2: C-V characteristics of germanide/SiO_2 gate stacked MOS capacitors.

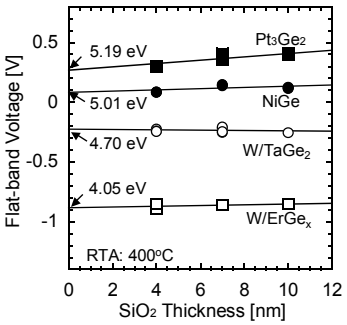

Fig. 3: Flat-band voltage of germanide gated MOS capacitors as a function of oxide thickness.

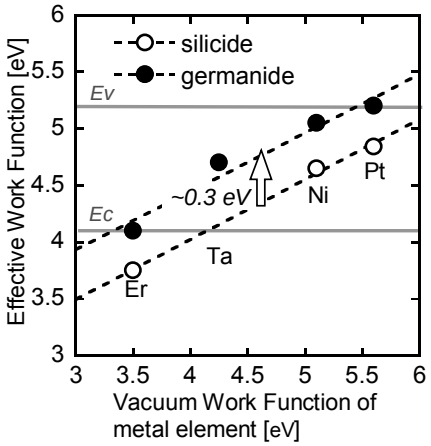

Fig. 4: Φ_{eff} value vs Φ_{vac} value of the metal element for germanides and silicides. PtSi and $ErSi_{1.7}$ were formed by co-sputtering of metal and Si, and NiSi formed by FUSI process.

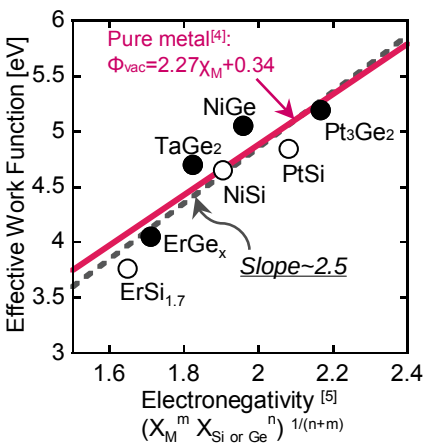

Fig. 5: Φ_{eff} value vs geometric mean of the metal and the silicon or germanium electronegativities. (m : n = Metal : Si(Ge))

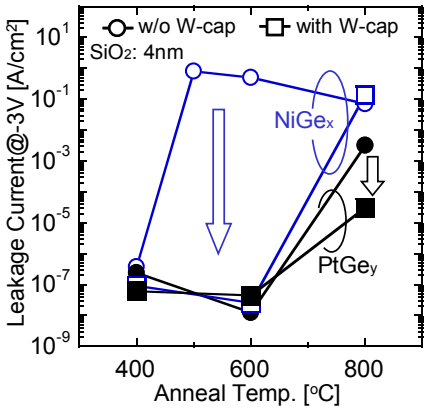

Fig. 6: Dependence of gate leakage current of germanide MIS capacitor with SiO_2 on annealing temperature with or without W-cap.

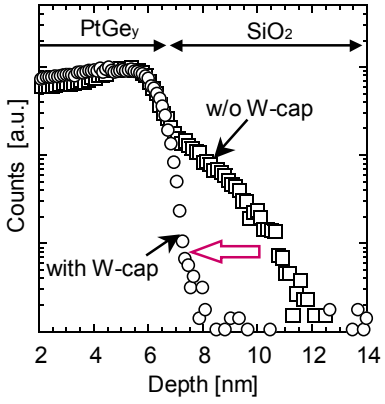

Fig. 7: Backside SIMS depth profiles of Ge after 800 °C annealing, in $PtGe_y/SiO_2$ with or without W-cap layer.

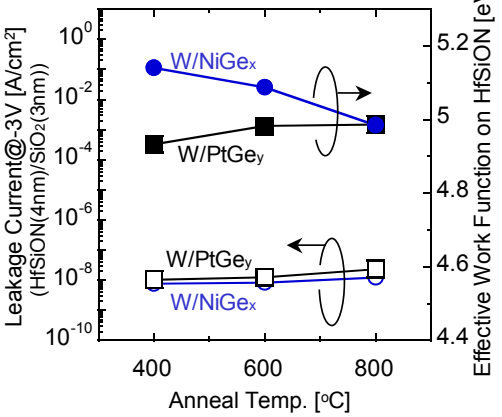

Fig. 8: Dependence of gate leakage current and Φ_{eff} value of germanide/HfSiON on annealing temperature.

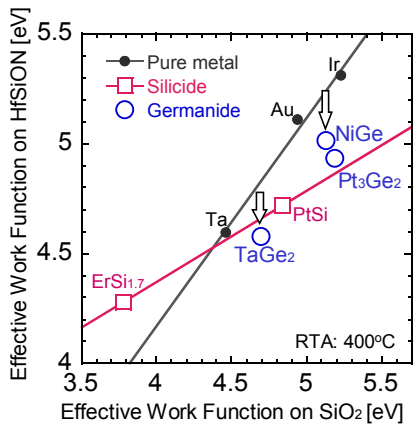

Fig. 9: Φ_{eff} value on HfSiON vs SiO_2. Pure metal gate electrodes were formed by sputtering.