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$Mo_XSi_YN_Z$ Metal Gate Electrode with Tunable Work Function for Advanced CMOS

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1. Introduction

The use of metal gate electrodes can overcome problems such as gate depletion and dopant penetration, associated with poly-silicon gate electrodes. For bulk CMOS devices, the work functions of metal gates should be close to those of n^+poly and p^+poly-Si [1]. Much work has been focusing on the dual metal gate approach to improve CMOS performance. Alloying and implantation are being considered as possible techniques to tune the metal gate work function, however, the Φ_{eff} appears to be stable only up to 800°C [2] [3]. The ternary, $TaSi_XN_Y$, has been investigated as a metal gate electrode. However, after RTA 900°C annealing, the Φ_{eff} increases to mid-gap level [4]. $Mo_XSi_YN_Z$ ("MoSiN") has been reported as an amorphous effective diffusion barrier for Al metallization [5]. In this paper, the work function tunability and thermal stability of reactively co-sputtered MoSiN metal electrodes are reported for the first time. Our results demonstrate that the work function of MoSiN can be tuned over a wide range suitable for both PMOS and NMOS by adjusting the deposition conditions and post annealing.

2. Experimental

Fig. 1 shows the MOS capacitor fabrication process flow. MoSiN films were deposited by reactive co-sputtering of Mo and Si targets in an Ar and N_2 ambient of 25 mTorr with a base pressure of ~5×10^{-9} Torr on thermally grown SiO_2. MoSiN film deposition parameters were listed in Table I. High frequency (100 KHz) Capacitance–Voltage (C-V) and Current-Voltage (J-V) characteristics were performed using a Keithley 590CV meter and a Keithley 4200 analyzer, respectively. In addition, Rutherford Backscattering Spectrometry (RBS) was performed to evaluate the composition and thermal stability of MoSiN films. X-ray Diffraction (XRD) was performed to identify the phase variation of the films with annealing temperature.

3. Results and Discussion

Fig. 2 shows examples of RBS spectra of as-deposited and annealed films. The compositions of as-deposited and annealed films determined by RBS simulation [6] are summarized in Fig. 3. For films with a high or low N concentration and a low Si content, we detect a N loss after 1000°C annealing, indicating that the thermal stability of MoSiN films depends on the Si and N concentration. By increasing the Si content in the films (e.g. sample 6), the composition of the films remains nearly constant even after 1000°C annealing, improving the thermal stability. Fig. 4 shows C-V for MOS capacitors with as-deposited MoSiN electrodes. The C-V curves continuously shift to positive voltages with increasing N concentration. The V_{FB} vs. SiO_2 thickness plot shown in Fig. 5 exhibits good linear relationships between V_{FB} and SiO_2 thickness for all stacks. Based on the Φ_{eff} extracted from Fig. 5, a $\Delta\Phi$~0.6eV "tuning window" is observed for as-deposited films. After high temperature annealing, the C-V characteristics depend on the film composition. Fig. 6 shows that the V_{FB} of sample 3 capacitors shifts to negative voltage values, particularly after 900°C anneal. The V_{FB} shows a good stability even after a 1000°C anneal, as well as an *additional* 1000°C 10s anneal. The linear relationships between V_{FB} and SiO_2 thickness are shown in Fig. 7 and the extracted Φ_{eff} is summarized in Fig. 9. After 900°C annealing, this film shows a stable Φ_{eff} ~4.3eV. As the Si content in the films increases, the C-V of the sample 6 electrodes shows better stability as shown in Fig. 8. The V_{FB} is almost the same with different temperature anneals and the extracted $\Phi_{eff}\approx$4.95eV is thermally stable up to 900°C as shown in Fig. 9. Fig. 10 shows that J-V curves for sample 3 under gate injection. The leakage current (@V_{FB} -1) remains nearly constant with annealing temperature. The Fowler-Nordheim tunneling barrier height was extracted from J-V curves (Fig. 10), and barrier height values correlate well to the extracted Φ_{eff} from C-V data (Fig. 11). XRD for sample 3 in Fig. 12 shows that the preferred orientation is not the close-packed (111) plane of cubic Mo_3N_2, but the less packed (200) plane, possibly corresponding to the low Φ_{eff}. It is noted that the peak position (42.6°) of the (200) plane of as-deposited films is less than the bulk value (43.418°) of cubic Mo_3N_2 (200), possibly because of the expansion of the lattice constant due to excessive N. After 900°C annealing, the peak position approaches the bulk values, possibly due to excessive N pile-up at the interface of $MoSiN/SiO_2$. The segregated N at the interface may result in the decrease of the Φ_{eff}. For MoSiN films (X=42%, Y=18%, Z=40%), which have more Si-N bonds in the films relative to other samples (e.g. sample 2, 4, and 5), there is no N loss even after 1000°C annealing, and the amorphous phase is thermally stable up to 900°C as shown in Fig. 12. Both effects likely contribute to a stable PMOS compatible work function.

4. Summary

We demonstrate that the work function of MoSiN films can be tuned ~0.7eV by adjusting the compositions of the films and post-annealing. By controlling the reactive co-sputtering conditions, a $Mo_XSi_YN_Z$ (X=46% Y=12%, Z=42%) gate presents an NMOS compatible $\Phi_{eff}\approx$4.3eV after 900°C annealing. By increasing Si content (X=42%, Y=18%, Z=40%), the $\Phi_{eff}\approx$4.95eV is compatible with PMOS and thermally stable up to 900°C. These results suggest that $Mo_XSi_YN_Z$ may be useful for fully depleted (SOI) dual Φ metal gate applications.

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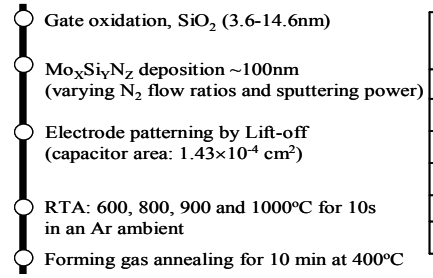

Fig. 1 The fabrication process of metal gate capacitors.

Table I Metal gate deposition parameters

sample	N_2 flow Ratio (N_2/(N_2+Ar))	DC power (Mo)	RF power (Si)
1	0%	100W	100W
2	15%	100W	100W
3	30%	100W	100W
4	50%	100W	100W
5	66.7%	100W	100W
6	30%	50W	150W

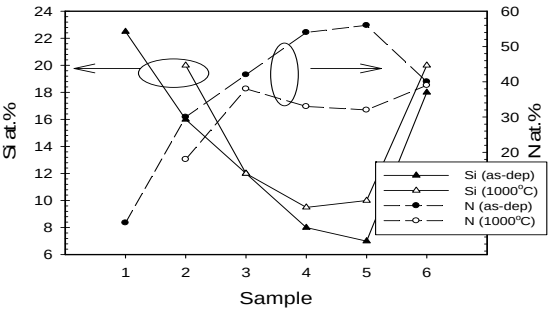

Fig. 3 The composition of as-deposited and annealed films.

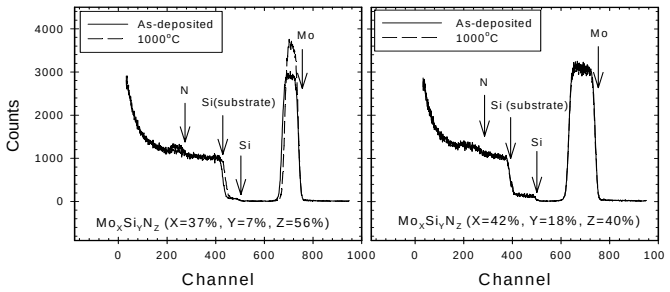

Fig. 2 RBS spectra of as-deposited and annealed MoSiN/Si.

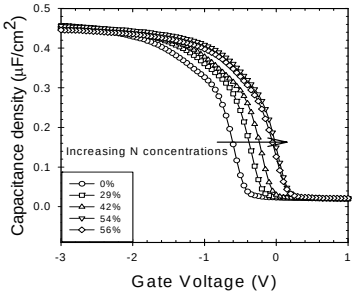

Fig. 4 C-V of as-deposited MoSiN Capacitors.

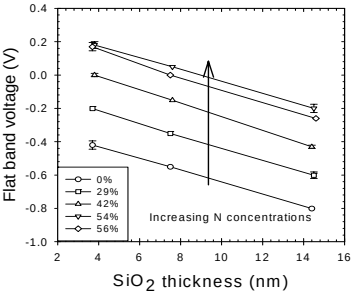

Fig. 5 V_{FB} vs. SiO_2 thickness for as-deposited MoSiN/SiO_2/Si capacitors.

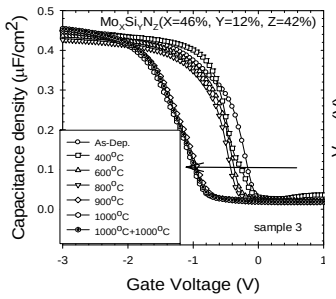

Fig. 6 Annealing effects on C-V of sample 3.

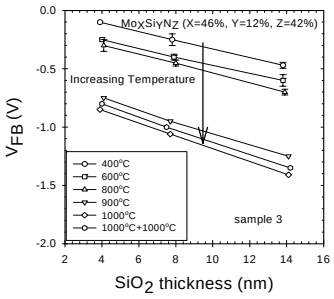

Fig. 7 V_{FB} vs. SiO_2 thickness for sample 3 with various anneals.

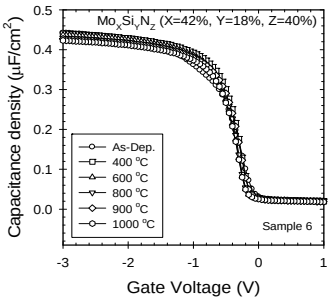

Fig. 8 Annealing effects on C-V of sample 6.

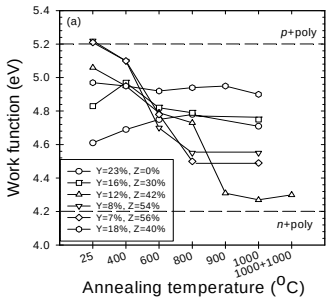

Fig. 9 Effective work function of MoSiN films with various anneals.

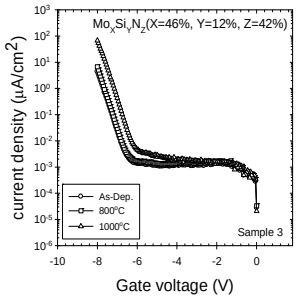

Fig. 10 J-V curves of sample 3.

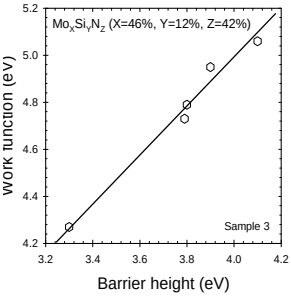

Fig. 11 Effective work function as a function of barrier height.

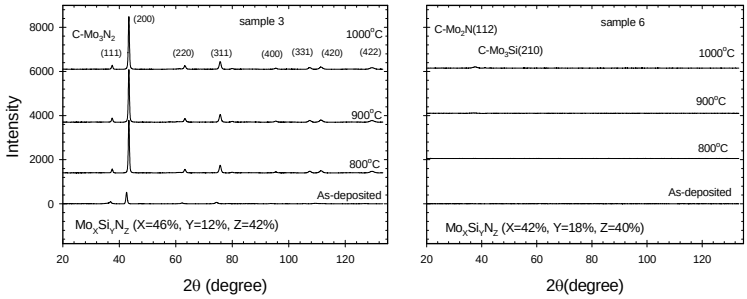

Fig. 12 XRD analysis of sample 3 and sample 6 with various anneals.