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Low temperature divided CVD technique for TiN metal gate electrodes of p-MISFETs

Shinsuke Sakashita, Kenichi Mori, Kazuki Tanaka*, Masaharu Mizutani, Masao Inoue,
Shinichi Yamanari, Jiro Yugami, Hiroshi Miyatake, and Masahiro Yoneda
Process Development Dept., Process Technology Development Div., Production and Technology Unit, Renesas Technology Corporation
*Process Engineering Section, Wafer Process Engineering Dept., Renesas Semiconductor Engineering Corporation
4-1, Mizuhara, Itami-shi, Hyogo, 664-0005, Japan
Phone: +81-72-784-7373 / Fax: +81-72-780-2756 / E-mail: sakashita.shinsuke@renesas.com

1. Introduction

High-k materials such as $HfSiO_x(N)$ and $HfAlO_x$ have been widely investigated and discussed as alternative gate dielectrics to SiON [1]. Among various high-k materials, HfSiON is one of the most promising candidates for 45 nm-node CMOS devices. However, a poly-Si/HfSiON gate stack brings about Fermi level pinning, which shifts the threshold voltage (V_{th}) of a MIS transistor and narrows the tuning range of V_{th}. In order to avoid Fermi level pinning as well as the depletion of the poly-Si electrode, a metal electrode is introduced concurrently with high-k gate dielectrics. As the V_{th} shift due to Fermi level pinning is more severe for p-MISFETs than n-MISFETs [2], a metal gate electrode which has a proper work function (Φ) for p-MISFETs ($\Phi \geq$~4.8eV) is a high priority.

In this work, as a candidate for a metal gate electrode, we focused on titanium nitride (TiN), which is widely used in LSI production, and found out that its effective work function (Φ_{eff}) can be controlled to an adequate value of 5.15eV (on HfSiON) for p-MISFETs by optimizing CVD condition.

2. Experiment

The electrical properties of TiN gate electrodes were evaluated with MIS capacitors. Figure 1 illustrates the structure of the MIS capacitors and the fabrication flow. A conventional SiON film and a HfSiON film formed by nitridation of MOCVD-HfSiO were used as the dielectric layers of the MIS capacitors. A CVD-TiN film for the gate electrode is deposited by using $TiCl_4$ and NH_3, followed by the deposition of a PVD-TiN film to reduce the resistance of the gate electrode. In this experiment, we applied two kinds of deposition methods for TiN-CVD. One is a conventional method which consists of a TiN deposition step and a post NH_3 anneal step for the reduction of the residual Cl in the film, and the other is a divided deposition method in which the combination of a TiN deposition step and a post NH_3 anneal step is repeated several times [3, 4]. A PVD-TiN gate electrode deposited by reactive sputtering was also evaluated for a comparison. Some samples received RTA treatments to evaluate the thermal stability of the TiN electrodes.

C-V and J-V characteristics were measured. The effective work function and EOT were calculated by using the EPOQUE program [5]. The surface morphology of the TiN films was observed by SEM and the bonding state was evaluated by EELS.

3. Results and Discussion

Figure 2 shows the C-V characteristics for the TiN gate electrodes formed on thick SiON gate dielectrics (SiON=20nm) by conventional CVD and PVD. The effective work function of the CVD-TiN electrode was calculated at 4.76eV, while 4.56eV was obtained for the PVD-TiN electrode. Figure 3 shows the J-V characteristics for the CVD-TiN and PVD-TiN electrodes on thin SiON gate dielectrics (SiON=1.8 nm). The gate leakage current density of the PVD-TiN electrode is much higher than that of CVD-TiN. This result indicates that the PVD method damages thin SiON dielectrics during deposition. Therefore a CVD method is more suitable for the gate stack formation of p-MISFETs.

The dependence of gate leakage current density on the deposition temperature of TiN-CVD is shown in Fig.4. The solid line shows the gate leakage current density of the divided CVD-TiN electrode, and the dashed line shows that of the conventional CVD-TiN electrode. Although the gate leakage current density decreases with lowered deposition temperature for both methods, the gate leakage current density of the divided CVD-TiN electrode is higher than that of the conventional CVD-TiN electrode at the deposition temperature of 500˚C. During a post NH_3 anneal, by-products such as NH_4Cl and HCl are produced by the reaction of NH_3 with residual Cl in TiN films. Compared to the conventional TiN-CVD method, the post NH_3 anneal is applied on a relatively thin TiN film in each cycle of the divided TiN CVD method. Therefore, by-products such as HCl could easily reach the gate dielectrics through the TiN film and cause damage, as illustrated in Fig. 5. However, the conventional TiN-CVD method has a crucial disadvantage. Figure 6(A) shows the surface morphology of a conventional CVD-TiN film deposited at 450˚C. Anomalous growth substances appeared in the TiN surface at low temperature range ($\leq$ 450˚C). Furthermore, the gate leakage current stops decreasing, even if the deposition temperature is lowered below 450˚C. These results indicate that it is difficult to keep the gate leakage current density low without the appearance of anomalous growth substances by using the conventional TiN-CVD method. On the other hand, no anomalous growth substances appear even at a deposition temperature of 350˚C with the divided TiN-CVD method, as shown in Fig. 6(B). As a result, we can achieve a low leakage current density with a divided CVD-TiN electrode deposited at 350˚C without the appearance of anomalous growth substances. As shown above, the divided CVD method is more suitable than the conventional method for the formation process of TiN electrodes.

For the further optimization of the divided TiN-CVD method, effective work function and gate leakage current density were evaluated under various conditions. These results are summarized in Fig. 7. We found out that many parameters such as deposition pressure and post NH_3 anneal time have an effect on work function and gate leakage current density. Figure 8 shows the C-V characteristics of the CVD-TiN electrode formed by the conventional CVD method and the divided CVD method after optimization. An effective work function of 5.10eV could be obtained with a gate leakage current of 1.9E-3 A/cm^2 at $|V_g$(gate voltage)$-V_{fb}$(flat band voltage)$|$=1V for SiON gate dielectrics under the optimized condition that the deposition temperature is 350˚C, $TiCl_4/NH_3$ ratio is 1, and CVD-TiN thickness is 20 nm.

The optimized divided CVD-TiN electrodes were applied on HfSiON gate dielectrics. Figure 9 shows the C-V characteristics for HfSiON as well as for SiON. The effective work function of the TiN electrode on HfSiON is calculated at 5.15eV, which is almost the same as for SiON and suitable for p-MISFETs. This result also indicates that Fermi level pinning can be suppressed by using divided CVD-TiN electrodes.

In order to evaluate the thermal stability of the gate stacks using divided CVD-TiN electrodes, the gate leakage current density and EOT were evaluated after several kinds of thermal treatments. The results are summarized in Fig. 10. For TiN/SiON stacks, the gate leakage current density drastically increased after 1s of RTA at 1000˚C. However, as shown in Fig. 11, the EELS Ti spectra from TiN electrodes show no significant changes after RTA at 1000˚C. Therefore, the increase of the gate leakage current density after RTA at 1000˚C most likely resulted from damage to the SiON gate dielectrics caused by diffusion of residual Cl in the TiN electrodes. For the TiN/HfSiON stacks, as the thermal treatment became severe, the gate leakage current density and EOT increased only slightly, and the effective work function gradually shifted toward mid-gap, as shown in Fig. 12. After 1s of RTA at 1000˚C, an effective work function of 4.83eV was obtained with a gate leakage current density of 1.7E-2 A/cm^2 at $|V_g-V_{fb}|$=1V. The TiN/HfSiON stacks still maintained suitable properties for p-MISFETs after RTA.

4. Conclusions

TiN metal gate electrodes were investigated. We found out that divided CVD-TiN electrodes are more suitable for p-MISFETs under optimized conditions. The effective work function of divided CVD-TiN electrodes deposited at 350˚C was 5.10eV on SiON gate dielectrics and 5.15eV on HfSiON keeping the low leakage current. Although effective work function shifted towards mid-gap after RTA at 1000˚C, the divided CVD-TiN electrodes still maintained suitable properties for p-MISFETs.

References

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[2] C. Hobbs et al., Symp. VLSI Tech., p9 (2003)
[3] S. Sakashita et al., SSDM, p762 (2004)
[4] T. Okudaira et al., JJAP (to be published)
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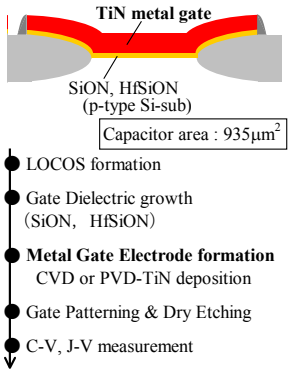

Fig.1 MIS capacitor structure and its formation flow.

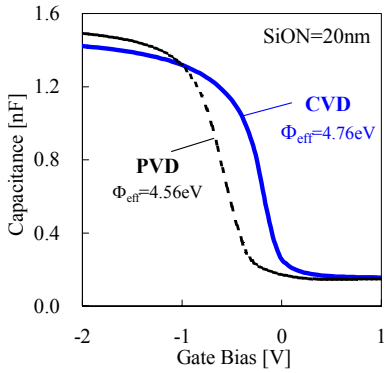

Fig. 2 C-V characteristics for thick SiON (= 20nm) capacitors with conventional CVD-TiN and PVD-TiN gate electrodes.

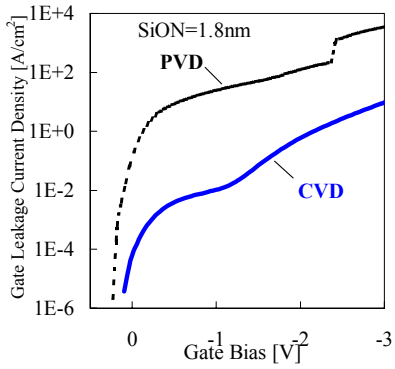

Fig. 3 J-V characteristics for thin SiON (= 1.8nm) capacitors with conventional CVD-TiN and PVD-TiN gate electrodes.

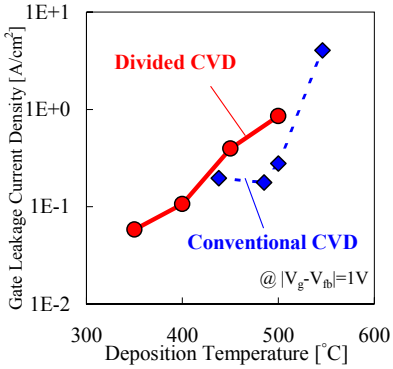

Fig. 4 Dependence of the gate leakage current density on the deposition temperature of CVD-TiN gate electrodes. The solid line shows divided CVD, and the dashed line shows conventional CVD.

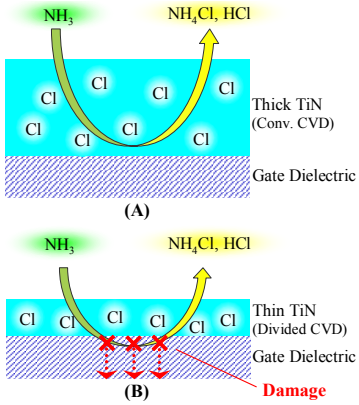

Fig. 5 Influence of NH_3 anneal processes. (A) For thick TiN films formed by conventional CVD. (B) For thin TiN films formed by divided CVD.

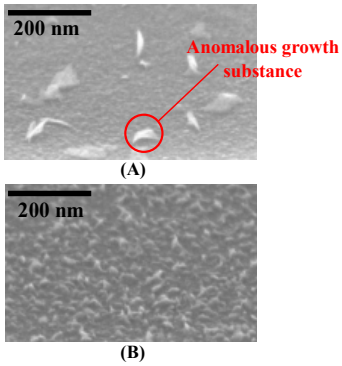

Fig. 6 SEM images of TiN surfaces. (A) Surface of the conventional TiN deposited at 450°C. Anomalous growth substances are observed. (B) Surface of the divided TiN deposited at 350°C. No anomalous growth substances are observed.

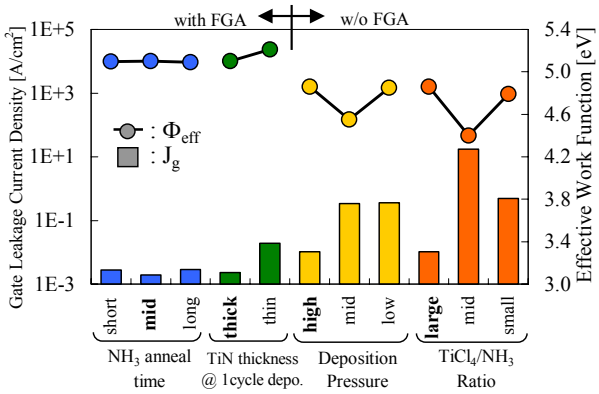

Fig. 7 Gate leakage current density @ $|V_g-V_{fb}|$=1V, and work function under various conditions of TiN-CVD. The parameters written by the bold-faced type were applied as the optimized condition.

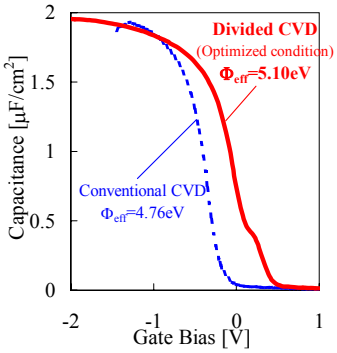

Fig. 8 C-V characteristics for SiON(=1.8nm) gate dielectrics. The solid line shows the optimized divided deposition TiN electrode. The dashed line shows the conventional TiN electrode.

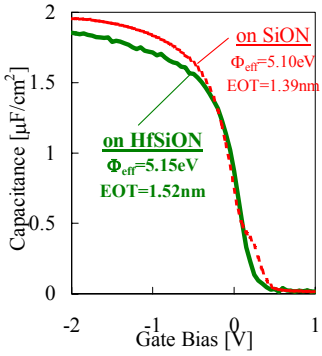

Fig. 9 C-V characteristics for optimized divided CVD-TiN electrode on HfSiON gate dielectrics (solid line), and on SiON (dashed line).

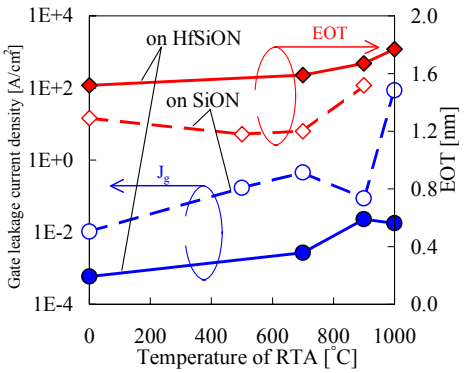

Fig. 10 Dependence of gate leakage current density and EOT on the temperature of RTA for TiN/HfSiON stacks (closed symbols) and TiN/SiON stacks (open symbols).

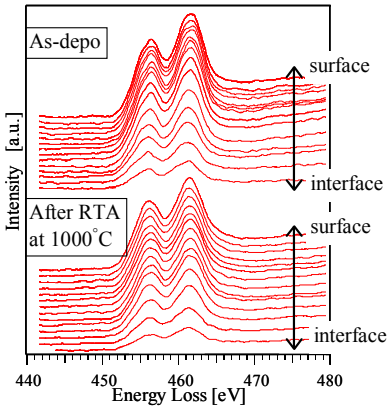

Fig. 11 EELS Ti spectra from TiN electrodes. No significant changes were observed after 1s of RTA at 1000°C.

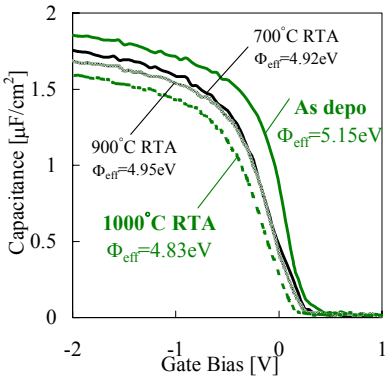

Fig. 12 C-V characteristics for TiN/HfSiON stacks after RTA under several conditions. Work function shifts to the mid-gap as the thermal treatment becomes severer. After 1s of RTA at 1000°C, a work function of 4.83eV was obtained.