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Influences of Activation Annealing on Characteristics of Ge p-MOSFET with ZrO_2 Gate Dielectric

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1. Introduction

Since the aggressive scaling of MOS devices leads to the fundamental limit of SiO_2 as the gate dielectrics, high-quality deposited high-k materials have been developing for the replacement of SiO_2. On the other hand, Ge is one of the attractive materials as the substrate of MOSFET due to its higher mobility compared to Si [1]. In particular p-channel Ge FET is desirable since bulk hole mobility of Ge is four times as high as that of Si and it can be enhanced furthermore by strain [2]. In order to realize both thin EOT and high drive current, high-k/Ge is one of the attractive combination and promising electrical characteristics on the high-k/Ge system have been reported recently [3]. Furthermore owing to the low-temperature dopant activation in the Ge substrate [3], high-k materials that react with Si at temperatures as high as 1000°C could be re-examined as the prospective candidates. We have already shown that ZrO_2/Ge gate stacks are more preferable to realize both thin EOT and low J_g than HfO_2/Ge ones [4, 5]. Although ZrO_2/Ge gate stacks have been already reported [3–7], so far little has been reported on the influences of activation annealing on Ge MOSFET device characteristics. The purpose of this work is to clarify the influence of the activation annealing on the characteristics of Ge p-MOSFET with ZrO_2 gate dielectric. Particularly, we address the issue of (i) interfacial layer (I. L.) thickness, (ii) gate leakage current, (iii) band alignment and (iv) activation annealing of p+/n-junction formation. Ge p-MOSFET performance is demonstrated with the optimized temperature.

2. Experimental

ZrO_2 was deposited by sputtering on (100) n-type Ge substrate (Sb: 0.05 Ωcm) which were cleaned with DHF (1%) and DI water rinse. Impurity activation annealing was performed at from 400 to 800°C for 30 min in N_2 after making gate electrode. Molybdenum was used for the gate electrode of MOS capacitor and p-MOSFETs. BF_2^+ (5 x 10^{15} cm^{-2}, 50 keV) was implanted to form p+/n-region. Forming gas annealing (H_2: 10%) was carried out for MOS capacitor and p-MOSFET at 350°C for 30 min. For the band gap measurement, thick ZrGeO insulators of 100 nm on Si substrate deposited by sputtering with Zr and Ge target were used for the reflection electron energy loss spectroscopy (REELS).

3. Results and Discussion

(i) Physical influences of annealing

Figures 1(a)–(d) show high-resolution cross-sectional transmission electron microscopy (HR-XTEM) images for the samples before and after annealing in N_2. The I. L. thickness decreased by the interdiffusion with ZrO_2 after 500°C annealing in N_2. The complete absence of the interfacial layer after 500°C annealing could be confirmed by the fact that the crystal lattice of ZrO_2 reached down to the surface of the Ge substrate, as shown in Fig. 1(d). As a result, Ge was incorporated into ZrO_2 above 500°C (Fig. 2), in which Ge concentration relative to Zr was about 15% inside high-k films. Since electrical properties could change as a result of the Ge incorporation into ZrO_2, we next investigated the influences of annealing on the electrical characteristics at the temperature as low as that needed to activate the dopant.

(ii) J_g, band alignment and activation of p+/n-junction

Figure 3 shows that gate leakage current density (J_g) remained as small as 1x10^{-7} A/cm^2 after annealing in N_2. Figures 4 show that band gaps (E_g) derived from REELS were almost the same up to Ge/(Ge+Zr)=50%. Since Ge/(Ge+Zr) ratio in ZrO_2 after 500°C annealing in N_2 was about 15%, E_g of the sample is also expected to be the same as as-deposited one. Figures 5 show that valence band offset (ΔE_v) between Ge incorporated ZrO_2 and Ge substrate, which is derived from valence XPS spectra of high-k and the substrate. ΔE_v was almost the same of 3.3 eV before and after 500°C annealing in N_2. Combining these results, band alignment didn't change after Ge incorporation into ZrO_2 film as depicted in Fig. 5(c). This is one of the reasons why no large gate leakage increase was observed with PDA [4, 5].

Next we investigated the activation of p+/n-junction. Figure 6 shows sheet resistivity (ρ_{sh}) derived from the regression for the sample measured by two-terminal method with different width as the inset in Fig. 6. From ρ_{sh} results, boron is expected to be highly activated above 400°C [3]. As shown in Fig. 7, the results of spreading resistance analyses (SRA) indicated the low temperature dopant activation [8]. The peak concentration (C_m) of electrically active dopant was 5x10^{19} cm^{-3}. Figure 8 shows J-V characteristics for the p+/n-junction. Samples annealed from 400°C to 600°C showed the good rectifying diode characteristics with the reverse leakage current below 10 mA/cm^2. The ratio between the forward biased current density (J_f) and the backward biased current density (J_b) reached around four orders of magnitude at the sample annealed at 500°C. It should be noted that temperature of 400°C is high enough for the activation of implanted dopant.

(iii) Characteristics of p-MOSFET

Below 500°C, the effect of annealing temperature on transistor characteristics was small: good cut-off characteristics were obtained (I_s-V_g, I_s-V_d for 500°C are shown in Figs. 9, 10). S-factor was as small as 80 mV/decade. Hole mobility (μ_h) of the ZrO_2/Ge gate stacks annealed at 500°C slightly increased compare to that at 400°C (Fig. 11). It was as high as 100 cm^2/Vsec at maximum and comparable to the reported hole mobility of HfO_2/Ge gate stacks with interfacial GeON layer [9]. Considering the complete disappearance of I. L. at 500°C, the mobility enhancement of the sample annealed at 500°C may indicate that the direct high-k/Ge interface is superior to the ZrO_2/I. L. (composed of GeO_x)/Ge interface.

4. Conclusion

ZrO_2/Ge gate stacks retained the structural integrity at Ge p-MOSFET fabrication process temperature of as high as 500°C. Band alignment for Ge incorporated ZrO_2 film on Ge didn't change compared to ZrO_2 on Ge. Good rectifying diode junction characteristics led to the promising p-MOSFET characteristics. Hole mobility of direct high-k/Ge gate stacks was as high as 100 cm^2/Vsec.

References

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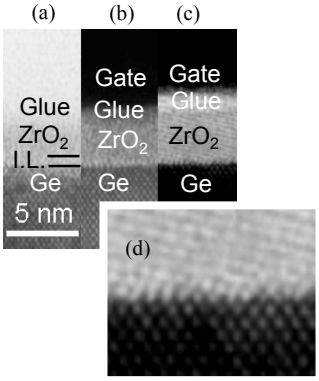

Fig. 1 HR-XTEM images of ZrO_2 / Ge (a)as-deposited, annealed at (b) 400°C and (c) 500°C. (d) is enlargement of (c).

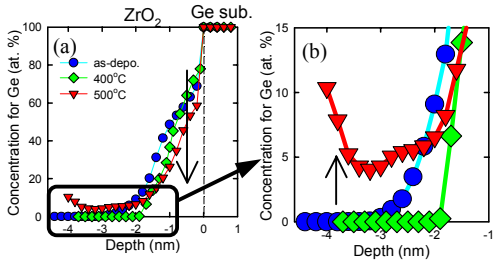

Fig. 2 (a) Depth profile of Ge atoms in ZrO_2 layer and (b) its enlargement. With PDA, Ge profile decreases in the interface region in (a) and Ge content in ZrO_2 increases after annealing at 500°C.

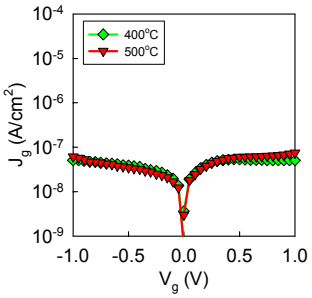

Fig. 3 J_g of Mo / ZrO_2 10nm / n-Ge.

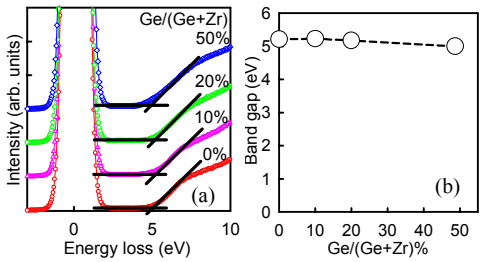

Fig. 4 (a) REELS spectra and (b) extracted E_g.

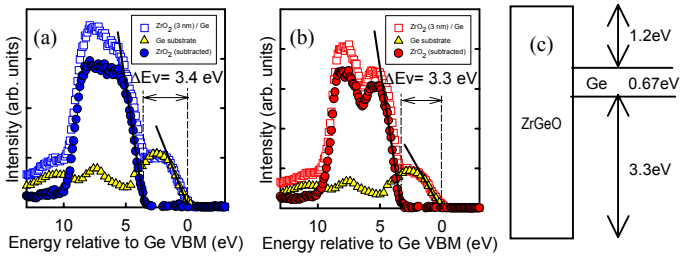

Fig. 5 Valence XPS spectra for ZrO_2 film on Ge (a) before and (b) after annealing at 500°C. The onset of valence spectra corresponds to valence band maximum (VBM). Valence band offset (Δ Ev) between ZrO_2 and Ge is derived from subtracting the spectrum of Ge substrate (triangle) from that of ZrO_2 on Ge (square). (c) Schematic diagram indicates band alignment for Ge incorporated ZrO_2 film on Ge.

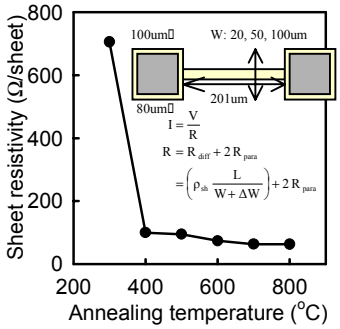

Fig. 6 Sheet resistivity (ρ_{sh}) dependence on anneal temperature. ρ_{sh} is derived from regression using 2-terminal measurement of the rectangle sample with different width.

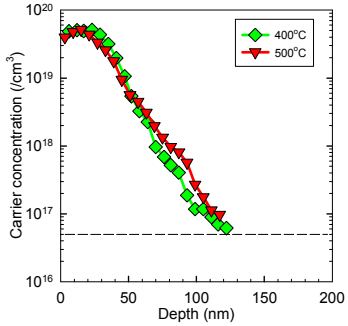

Fig. 7 Carrier concentration derived from spreading resistance analyses (SRA). Carrier concentration of substrate of $5x10^{16}$ ($/cm^3$) is also shown by dashed line.

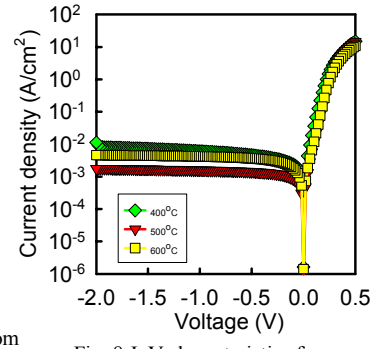

Fig. 8 J–V characteristics for p+/n diodes formed at various annealing temperatures.

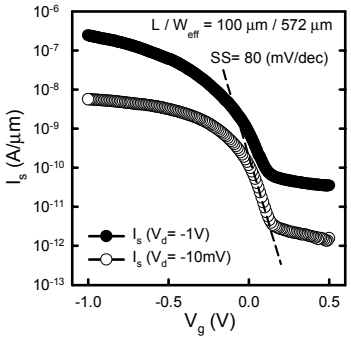

Fig. 9 V_g-I_s characteristics of the sample annealed at 500°C.

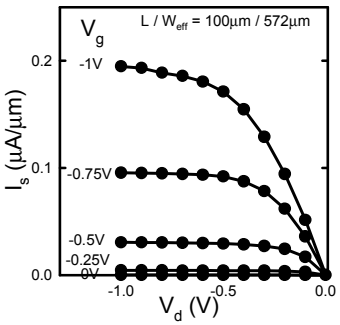

Fig. 10 V_d-I_s characteristics of the sample annealed at 500°C.

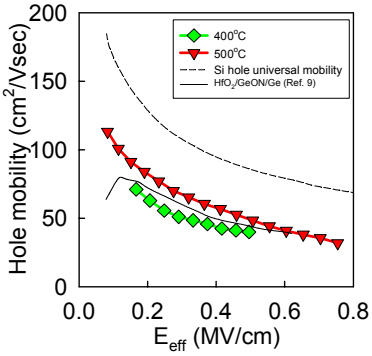

Fig. 11 Effective hole mobility.