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45nm Conventional Bulk and "Bulk+" Architectures for Low-Cost GP/LP Applications

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Abstract

In this paper, we discuss the scalability of Bulk architectures related to the 45nm CMOS generation. We show how the use of performance boosters can extend the bulk architecture for ultra-low cost applications and how performance can be even more improved by using bulk compatible architecture solutions such as "Silicon On Nothing".

Introduction

Static leakage management appears as a major roadblock in device design for the 45nm node. Indeed, the usual device "scaling rule" imposes a SiON gate oxide thickness responsible for a too high leakage in General Purpose (GP) or Low Power (LP) applications. A first solution is the use of High-K dielectrics. Nevertheless, their lack of compatibility with poly-Si gates imposes the use of dual-metal gates [1], requiring new materials or buried conduction channel [2-3], leading to strong DIBL. A first alternative is to minimize the scaling of gate oxide as proposed in [4] by keeping either Poly-Si gate or Single Metal Gate. In the first case, the subsequent loss on device speed performance is evaluated to 20% (Fig.1). Therefore, smart optimisation of device must be performed in order to compensate this speed degradation due to the static leakage reduction. Nevertheless, this conventional "Bulk" option is compatible with consumer electronics applications where a very low-cost is a major driver. The second choice implies using a mid-gap (or close to mid-gap) metal gate in combination with a fully depleted thin-film channel. This ensures the adjustment of threshold voltage for both GP and LP applications and allows a better scaling of total gate capacitance, by suppression of poly-depletion effects. A major point in this approach is the co-integration of regular bulk devices, in order to ensure a full compatibility of the I/O platform. The "Silicon On Nothing" (SON) architecture is a promising candidate in this perspective, defining a "Bulk+" architecture. In this paper we show examples of conventional "Bulk" optimisation using Strain-Silicon, advanced USJ and "Bulk+" integration for 45nm node.

Bulk optimisation for 45nm node

In order to compensate performance reduction due to gate stack limited scaling, the use of cumulated strained-silicon options is mandatory. For electrons, uni-axial tensile stress is known to allow performance improvement. This stress can be induced by a tensile nitride liner, used as Contact Etch Stop Layer (CESL) [5] as shown in Fig. 4, but other solutions can also be used, such as re-crystallization of the poly-Si gate under a capping layer (known as Stress Memory Technique – SMT [6]). The combination of both CESL and SMT can be achieved, and leads to an improvement of nMOS performance of 20% (Fig. 5). For holes mobility improvement, compressive liner can be used and co-integrated with tensile liner [7]. Nevertheless, a lower cost solution can be used for GP/LP application. Indeed, a closer view on the band structure of holes reveals anisotropy of the Heavy-Holes (HH) band (Fig. 4). In particular, HH are 'lighter' in the (100) direction. Therefore, using (100) channel for pMOS devices leads to 15% improvement on the saturation current (fig. 5). Integration of these conventional strained bulk devices with Lg=30nm (Fig. 3) into 0.334µm² SRAM bit-cells is shown in Fig. 6 [8]. Optimisation of USJ in order to achieve a good control of SCE and improved access resistance is also mandatory. Ultra short non-diffusing anneals are a promising candidates to realize both improvement of SCE control and dopant activation enhancement. As shown on fig 7, the combination of these new techniques (LSA or Flash Annealing) with spike annealing allows improving the nMOS (pMOS) performance by 11% (6%) respectively. Without spike annealing the DIBL effect can be significantly reduced for both nMOS and pMOS..

Bulk+ for 45nm node

The use of a modulated mid-gap metal gate in combination with fully depleted thin film is a way to obtain a regular gate capacitance scaling without static leakage degradation, and adjusted threshold voltages for both GP and LP applications. In one hand, slightly modulated mid-gap metal gates can be achieved by the use of the Totally Silicided (ToSi) gate process [9] using NiSi. Fig. 8 shows a TEM picture and performances of such devices.

In the other hand, the realisation of FD device on bulk substrates has been successfully demonstrated by using the Silicon On Nothing (SON) technique [10-11]. Fig 9 and 10 show the comparison of Lg=45nm poly-gate/SiON devices integrated with bulk and SON. Using thin films allows improving DIBL and SS and also using lightly doped channel. This leads to a measured current gain close to 30% at the same Vg-Vth. Moreover, using thin films allows a lower channel implantation, leading to a reduction of the junction leakage by 1 decade. This makes the SON well adapted for LP options. The co-integration of SON devices with regular bulk devices (such as I/O) can be achieved; and allows keeping existing design libraries when FD film are not wanted. Full co-integrated functional bulk and SON devices using poly-Si gates are shown in Fig. 11. This co-integration is achieved by protecting the Bulk zone from SiGe epitaxy that is used to define the SON Areas. Finally, the combination of the ToSi process with the SON process (Fig. 12) allows fabricating Bulk+ devices with adjusted threshold, scaled inversion capacitance, and improved subthreshold characteristics .

Conclusion

Using technological boosters, Bulk architecture is still a good candidate for low-cost consumer electronics products. Performance improved Bulk+ platform can be achieved by using combination of mid gap metal gate by ToSi process and Silicon On Noting technology.

Acknowlegment

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Reference :

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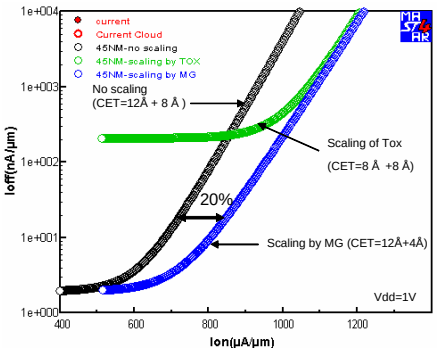

Fig.1 : Simulated Impact of gate oxide choice on device performances, using MASTAR4

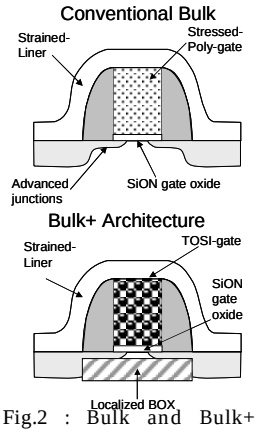

Fig.2 : Bulk and Bulk+ devices architecture

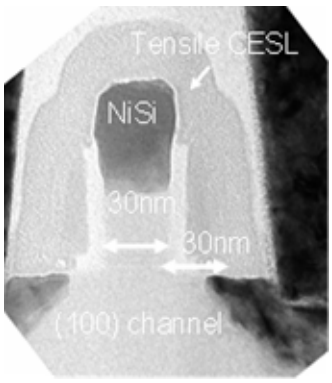

Fig. 3 : TEM Cross section of Bulk (L=30nm) with mobility boosters

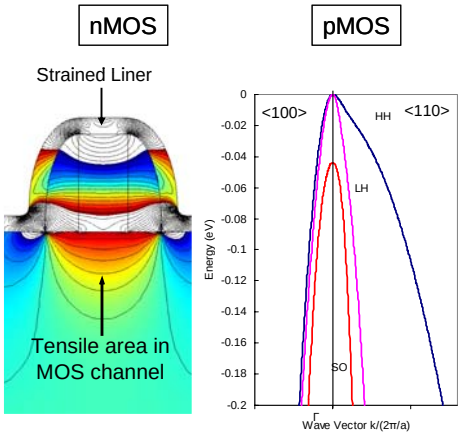

Fig. 4 :Mobility enhancement boosters for nMOS – strained liner and pMOS – 100 channel

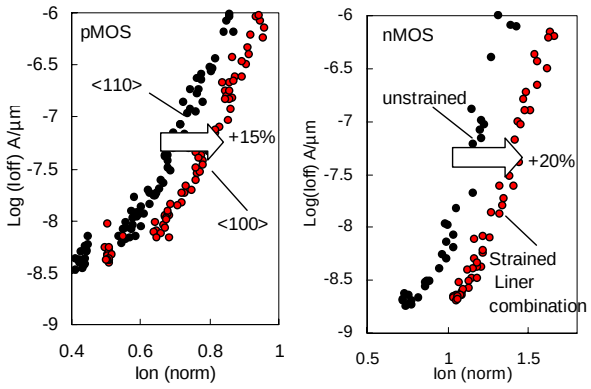

Fig. 5 : Impact of mobility enhancement technique of device performance. 15% and 20% improvement on Ion is achieved on pMOS and nMOS

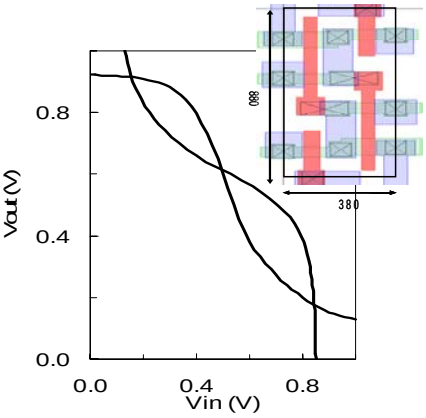

Fig. 6 : functional 0.334µm² SRAM bit-cell using Lg=30nm strained MOSFETS (Vdd=1.0V, SNM=114mV)

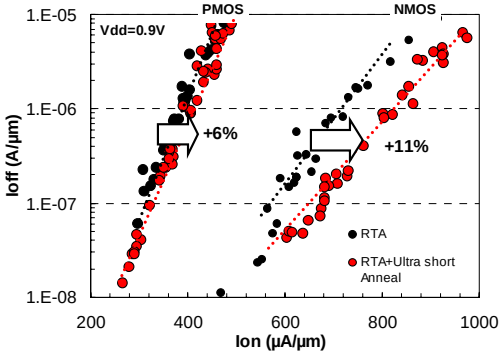

Fig.7 : Improvement of device performance using rapid annealing techniques (Vdd=0.9V)

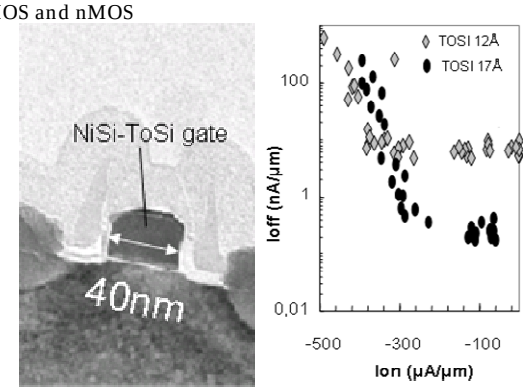

Fig.8 : TEM Cross-section and performance of ToSi gate pMOS devices (Vdd=1.2V)

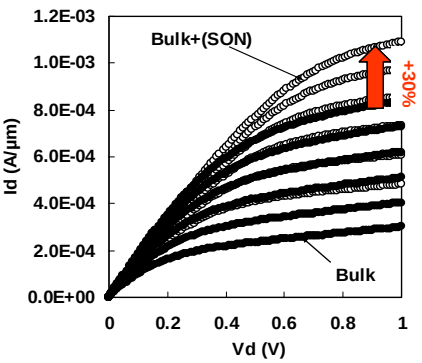

Fig 9: Bulk and Bulk+ (SON) saturation current at same Vg-Vth. 30% improvement is obtained using SON.

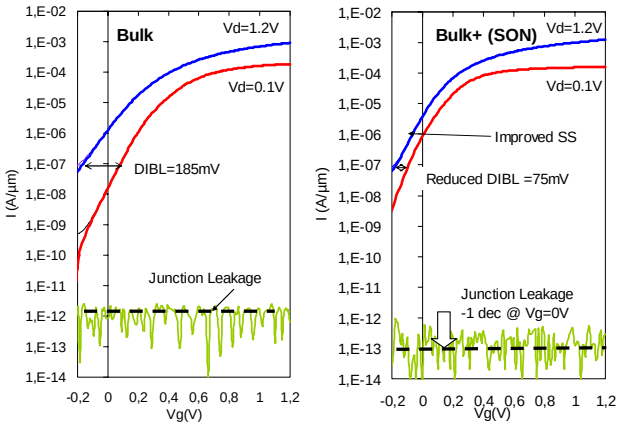

Fig. 10 : Bulk and Bulk+ (SON) with Poly/SiON subthreshold devices characteristic comparison (Lg=45nm). DIBL is reduced from 185mV down to 75mV,

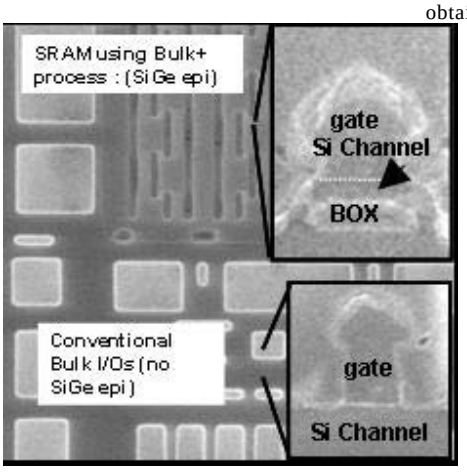

Fig. 11 : Co-integrated SON and regular Bulk devices into the same chip. SRAM are fabricated using SON and I/O are using Bulk.

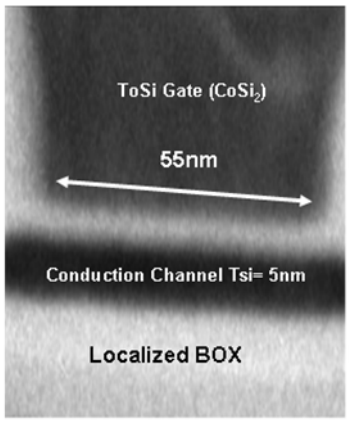

Fig. 12 : Example of co-integration of ToSi gate (here CoSi2) with SON module (Tsi=5nm)