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# A 90nm Hybrid SOI CMOS Technology Integrating PDSOI and Bulk Devices for Bulk-designed MPU Performance Booster

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**Abstract**

We have developed 90-nm node hybrid SOI CMOS technology that integrates PDSOI and bulk device to boost bulk-designed MPU performance. We have successfully obtained the same gate-length CD in both PDSOI and bulk regions. The key is the combination of modified SIMOX and optimized STI formation process which resolved the height difference and defects problem between PDSOI and bulk. Logic circuit speed and SRAM soft error immunity in PDSOI region improved dramatically: logic speed enhancement of 20% and SRAM error rate reduction of approximately two orders of magnitude. In addition, analogs and high-voltage I/O in bulk region maintained robust characteristics unaffected by the hybrid SOI process. We have fabricated bulk-designed microprocessor using this hybrid SOI technology, and obtained fully-functional chip.

## Introduction

Partially depleted (PD) SOI is a very promising technology for device performance improvement due to smaller junction capacitance and floating body effect. Especially, floating body enables high-speed operation with enhanced drive current and reduced body-bias effect. However, floating body effect also induces hump in DC on-current characteristics and history effect in AC operation, which pose huge impediment on precision-required circuit designs such as analogs. Therefore enormous amount of circuit and layout modification from bulk-based design is required for utilizing PDSOI devices.

In this paper, we describe 90-nm node SOI CMOS technology for bulk-designed MPU performance boost without circuit and layout modifications. In order to resolve the floating-body issue, we developed hybrid SOI process. PDSOI CMOS is applied for logic and SRAM cell, while bulk is used for PLL, SRAM sense amplifier, and high-voltage I/O as shown in Fig.1. We have compared PDSOI with bulk CMOS in terms of transistor characteristics, circuit performance, SRAM static noise margin and soft error immunity, and ESD immunity.

## Device Fabrication

In order to fabricate functional devices on both PDSOI and bulk region, we have developed the integration process that can achieve 1) reduction of the height difference between SOI and bulk region 2) removal of crystal defects at the border. Fig. 2 shows our process flow of hybrid SOI and STI formation. The height difference, which exceeded 2000 Å, has been reduced to less than 200 Å by optimizing SIMOX implantation and ITOX anneal process [1]. We have also carefully designed SOI-bulk boundary position, considering the BOX layer contraction and STI coverage. With this measure, crystal defects generated at the boundary are etched by STI formation. We have found that 1.5um width STI between SOI and bulk region was sufficient for crystal defect removal. In case of thermal liner oxidation is performed on STI reaching BOX layer, larger stress is generated at SOI/BOX interface leading to Tr. Characteristics degradation. To avoid this issue, dual STI process was developed as shown in Fig.2 [2]. First, shallow trench not reaching BOX layer was formed followed by thermal liner oxidation. Next, sidewall spacer was formed. Then, deeper trench, self-aligned with the shallow trench isolation by sidewall spacer, was formed. Transistor fabrication process after STI formation was basically the same as 90-nm node bulk CMOS technology with 45nm gate length transistor and Ni silicidation. With NiSi process technology we have developed [3], thin-body SOI device can be integrated without any issues.

We have fabricated bulk-designed microprocessor using this hybrid SOI technology, and obtained fully-functional chip. Fig. 4(a) shows the SEM view of the integrated microprocessor and, (b) and (c) show the TEM views of bulk CMOS transistor and SOI CMOS transistor, respectively.

## Transistor and Circuit Performance

Fig. 5 compares Ion/Ioff characteristics of the PDSOI Tr. and bulk Tr. formed on hybrid SOI wafer and conventional bulk wafer. In order to alleviate floating-body in PDSOI, we perform Ge implantation into body region which effectively suppress charge accumulation in neutral body region [4].As the result, the Ion-Ioff characteristic of 45nm gate length PDSOI MOSFET was almost the same as that of bulk MOSFET. We also confirm that the characteristic of bulk MOSFET was the same as that of bulk MOSFET on a conventional bulk wafer. From these result, bulk-designed circuit is expected to function on hybrid SOI without any special modification.

Fig. 6 shows correlation of MPU frequency with inverter gate propagation of high-speed logic circuit. Obvious correlation can be seen between inverter gate propagation delay and MPU frequency. Hybrid SOI, where high speed logic circuit is formed in PDSOI region, achieved 20% speed enhancement of inverter gate and 10% MPU frequency boost.

## SRAM Characteristics

Fig. 7 shows butterfly curves of SRAM cells with PDSOI and bulk device. Fig. 8 shows Static noise margin (SNM) vs. SRAM cell current. SNM of PDSOI is larger than bulk for the same cell current. This means that in case of PDSOI SRAM, larger cell current can be adopted to achieve faster SRAM operation compared with bulk without sacrificing SNM. In addition, Alpha-particle induced Soft Error Rate (SER) was compared between PDSOI and bulk at various alpha-particle energy as shown in Fig. 9. Correlation between SER and alpha-particle energy was observed in bulk devices but not in the case of PDSOI devices. PDSOI SER immunity is clearly improved, due to BOX layer preventing generated electron-hole pairs penetrating to SOI layer. PDSOI showed 70 times smaller SER than bulk at 6.9MeV.

## ESD Immunity

Figs. 10 and 11 show electrostatic discharge (ESD) failure voltage of PDSOI and bulk devices. As compared with bulk devices, SOI devices show much lower ESD immunity, although the failure voltages satisfies standard ESD criteria (Machine Model of 200V and Human Body Model of 2000V). This is mainly attributed to the poor heat conduction of buried-oxide layer. To improve PDSOI ESD immunity itself, enormous amount of circuit and layout modification may be required.

## Conclusion

We developed 90-nm node hybrid SOI CMOS technology that enables integration of PDSOI and bulk devices. Furthermore, we have applied this technology to existing bulk-designed microprocessor, in which high speed circuit and SRAM cell are formed in PDSOI region, while analogs and high-voltage I/Os are formed in bulk region. Fully functional chip of enhanced performance has been obtained with no circuit modification. This is a very effective method for MPU performance boost, free from any circuit and layout redesigns.

## Acknowledgements

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**References**

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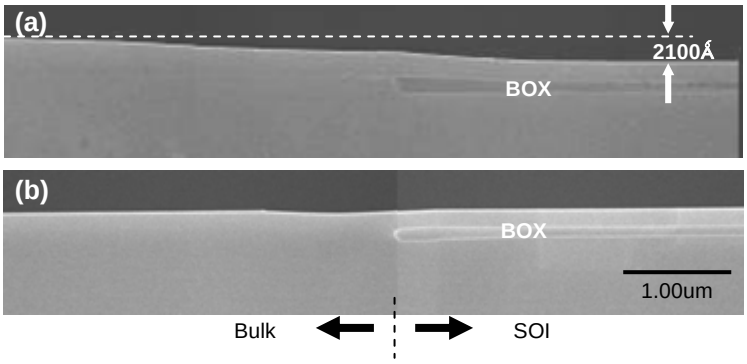


Fig.3 SEM cross sectional views of hybrid SOI substrate fabricated by (a) Control process and (b) optimized SIMOX process

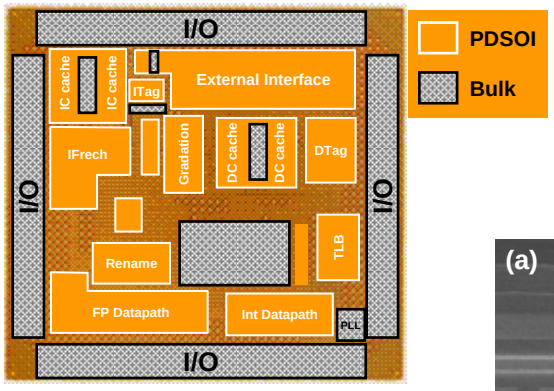


Fig.1 MPU Layout designed with PDSOI and Bulk.

- Hard mask SiO2 film deposition and lithography
- Hard mask etch
- SIMOX SOI fabrication
- Field nitride hard mask film deposition and lithography
- Field nitride hard mask etch and 1st STI etch
- Liner oxidation
- 2nd STI etch
- SiO2 deposition and CMP

Fig.2 Process flow of hybrid SOI and STI fabrication.

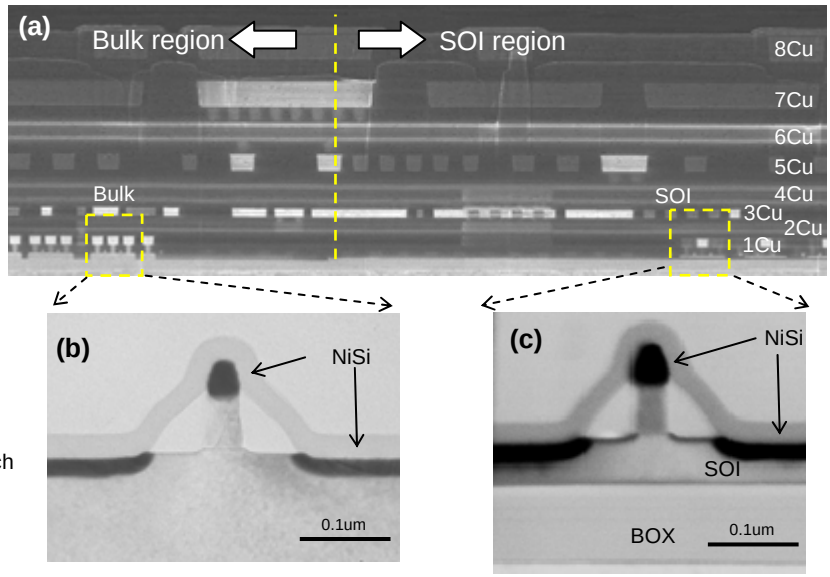


Fig.4 (a) SEM View of the MPU with sub-45nm gate, NiSi and 8Cu-layer, (b) TEM View of bulk Transistor, and (c) TEM view of PDSOI Transistor.

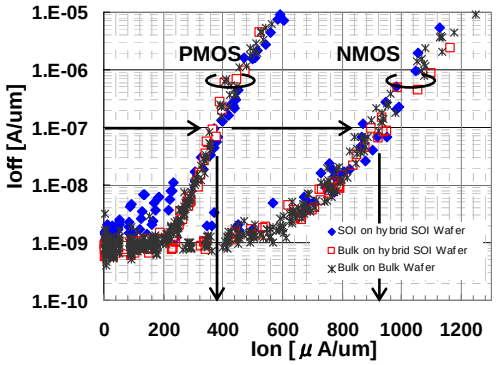


Fig.5 Ion/Ioff characteristics at Vdd=1.0V of PDSOI and Bulk

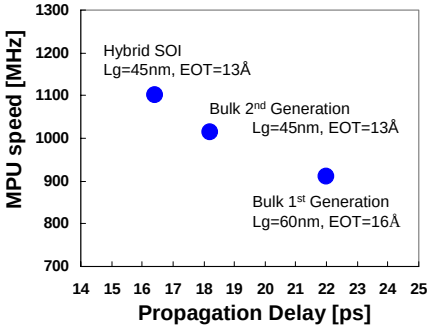


Fig.6 MPU speed vs Propagation delays of inverter gate (F/O=3).

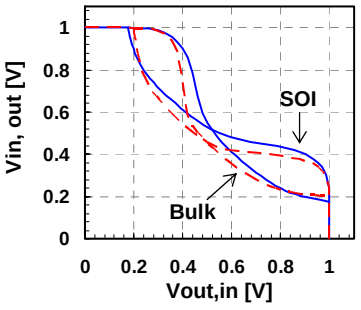


Fig.7 Butterfly curves of SRAM cells with PDSOI and Bulk.

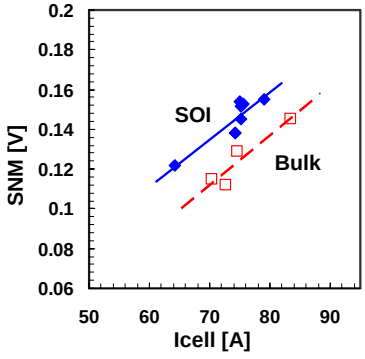


Fig.8 Static noise margin (SNM) vs. cell current of PDSOI and bulk.

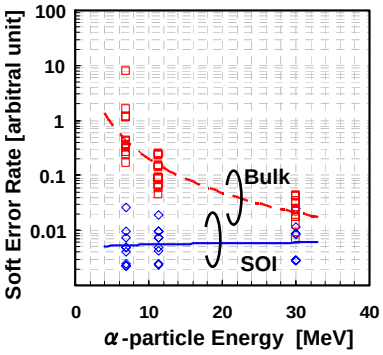


Fig.9 Alpha-particle induced Soft Error Rate (SER) of PDSOI and Bulk.

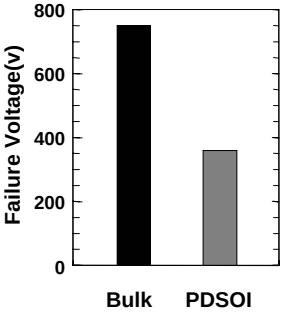


Fig. 10 Machine model failure voltage

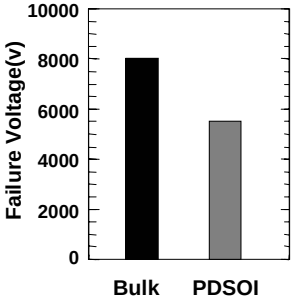


Fig. 11 Human body model failure voltage