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Effect of Process Induced Strain in 35 nm FDSOI Devices with Ultra-Thin Silicon Channels

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1. Introduction

The Fully-Depleted (FD) Silicon On Insulator (SOI) MOSFET is very promising for scaled CMOS technology generations. It provides an ideal subthreshold slope (~60mV/dec), reduced junction capacitances and a better control of short channel effects (SCE, DIBL). In addition, recent studies have successfully demonstrated that carrier transport properties are enhanced by applying an adapted strain to the conduction channel [1-3]. Integrated into CMOS bulk technology, the Process Induced Strained (PIS) is a low cost approach to boost the CMOS performances [4]. This can achieved by increasing the intrinsic stress of the so-called "Contact Etch Stop Layer" (CESL), in order to induce stress in the Si-channel [5,6]. Many publications on FDSOI devices have already been reported in the literature [7,8]. However their compatibility with a PIS approach has not been demonstrated. In this work, we propose to study the impact of a PIS approach on ultra-thin FDSOI devices down to L_g=35 nm. Based on the analysis of electrical results combined with mechanical simulations, we show that significant enhancement on both nMOS and pMOS can be achieved.

2. Mechanical Simulations

Finite elements simulations using ANSYS have been performed to model the mechanical stress transmission from the strained CESL to the channel and to understand the impact of this nitride layer on the channel transport properties in a FDSOI device. The 3D study was limited to an elastic behavior and considered that the device is free from stress before the SiN deposition, in order to analyze the contribution from the strained liner only. Isolated transistors with a 120 nm high poly gate associated with a 100 nm tensile (1.2GPa) CESL have been simulated. Even though a raised (25 nm) Source/Drain architecture was used, the stress is effectively transferred from the CESL to the underlying channel. Significant values of stress components are found (fig.1). These results also highlight that the stress level is strongly dependent on the layout (W and L_g). Two contributions of the strain are extracted in the channel: a central area (central effects) with a compressive strain and an edge area (edge effects) with a tensile strain. Edge effects are dominant for short devices whereas the stress becomes less tensile for longer devices. In order to compare the CESL effect in bulk and SOI devices, the Buried OXide (BOX) under the channel was replaced by a silicon layer. Due to the lower Young modulus of the BOX, the average in-plane stress intensity in the channel of the SOI device is increased compared to bulk devices (fig.2).

3. Experimental Results & Discussion

Process flow: nMOS and pMOS thin film SOI transistors were fabricated on 300 mm <100> UNIBOND™ SOI wafers with a BOX of 145 nm. SOI films were thinned down by thermal oxidation and wet etching to achieve a final thickness of around 10 nm under the gate at the end of the process. After STI isolation, a nitrided gate oxide dielectric is grown around 1.1 nm. A poly-Si layer of 120 nm was deposited for gate fabrication. A 193 nm lithography combined with trimming is realized to achieve reduced gate dimensions. After extensions/pockets implantations and spacer formation, a selective epitaxy of 15 nm is realized in order to facilitate NiSi S/D silicidation. A tensile or compressive CESL was deposited over both nMOS and pMOS. A cross sectional TEM picture of the final 35 nm FDSOI devices is shown in fig.3. Table 1 summarizes the features of the different CESL device variants.

CESL impact on performances: $I_d(V_d)$ characteristics are presented in fig.4 for 35 nm nMOS and pMOS. The best $I_d(V_g)$ curves measured on short devices are shown in fig.5. Figure 6 highlights for nMOS devices a 10.5% I_{on} improvement at I_{off}=100 nA/µm for a 100 nm tensile liner of 1.2 GPa versus no stress liner and a loss of 10% for a compressive strain. For pMOS devices, the use of a -1.8 GPa compressive stress versus low tensile stress (550 MPa) improve the performance by 17 % (fig.7). No significant threshold voltage variation for long transistor is measured (fig.8). This demonstrates a good control of the channel thickness (T_{Si}) uniformity between wafers. Similarly, extracted values of silicided and non silicided active area resistance (fig.9) or parasitic series resistance (not shown) confirm no difference between wafers. Therefore performance improvement can be attributed only to the enhancement induced by the strain influence.

Layout impact on CESL effect: we demonstrate the CESL impact down to very short gate length (fig.10). Figures 11 and 12 present the same trend on the linear G_m evolution. We note no significant G_m and I_{on} improvement for long channel (Lg> 1µm). For very short L_g, a significant gain in G_m is observed with a tensile CESL for nMOS (17%) compared to no stress CESL. With a compressive CESL on pMOS, a gain of 66% is obtained compared to a low tensile stress. If we now focus on the W impact, we show that the CESL effect for short channel (L_g=45 nm) nMOS devices remains constant for all W considered here (fig.13), excepted for the tensile liner case where G_m increases up to 38.5% as the W value decreases, as already observed for the bulk case [9]. However no major gain is obtained on pMOS devices, also confirmed in [9].

4. Conclusion

In this paper, we have shown that significant performance enhancements can be achieved by using the CESL approach on 35 nm gate length FD SOI devices. Performance enhancement up to 10% using a tensile liner for the nMOS and 17% using a compressive liner for the pMOS were obtained. As demonstrated, the strain level in the channel is very dependent on both gate length and device width. The combination of the advantages of FDSOI device with CESL technique can be a very interesting and promising solution for performance enhancements for the next device generations.

Acknowledgements
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Reference:

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[2] S. Thompson et al., IEDM 2002
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[6] C.Diaz et al., IEDM 2003
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[9] C. Ortolland et al., ESSDERC 2004

Devices	Strain	SiN Thickness
nMOS	0 MPa reference	100 nm
nMOS	+1.2 GPa high tensile	100 nm
nMOS pMOS	-1.8 GPa high compressive	100 nm
pMOS	+ 550 MPa low tensile	35 nm

Table 1: Summary of the different Contact Etch Stop Layer variants, with T_{Si}= 12 nm, T_{ox}= 1.1 nm and T_{BOX}= 145 nm.

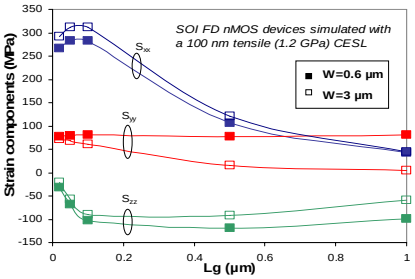


Figure 1: 3D simulation of strain components versus L_g for T_{Si}=10 nm, T_{BOX}= 145 nm and 25 nm raised S/D.

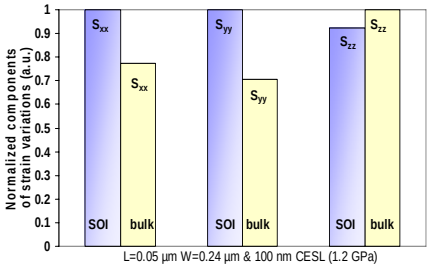


Figure 2: Stress impact between FDSOI and bulk on strain components with 25 nm raised S/D.

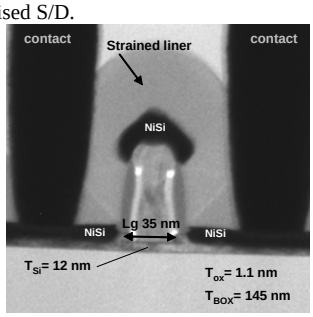


Figure 3: TEM cross-section of 35 nm nMOS FDSOI transistor with T_{Si}=12 nm, T_{ox}=1.1 nm and T_{BOX}= 145 nm.

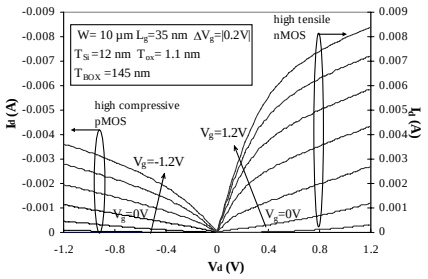


Figure 4: $I_d(V_d)$ curves for 35 nm nMOS (with high tensile strain) and 35 nm pMOS (with high compressive).

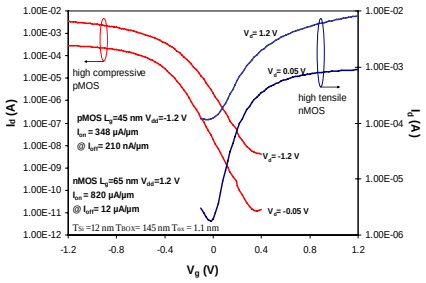


Figure 5: $I_d(V_g)$ curves for nMOS (with high tensile strain) and pMOS (with high compressive).

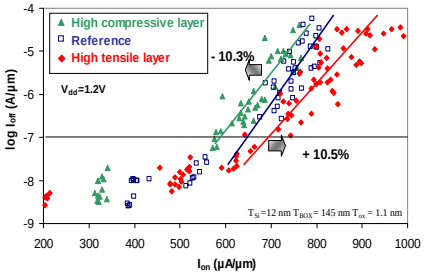


Figure 6: Impact of strained CESL on I_{on}/I_{off} characteristics at V_{dd}=1.2V for nMOS devices.

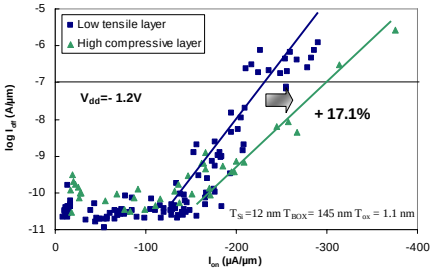
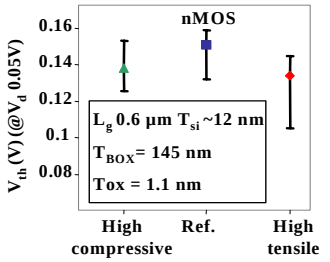


Figure 7: Impact of strained CESL on I_{on}/I_{off} characteristics at V_{dd}=-1.2V for pMOS devices.



igure 8: Long transistor linear V_{th} variations versus strained and no strained wafers.

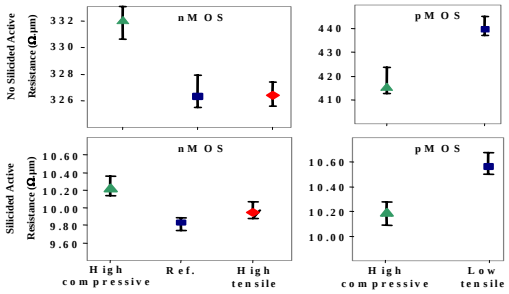


Figure 9: Comparison of SD silicided and no silicided resistances, with T_{Si}=12 nm, T_{ox}=1.1 nm and T_{BOX}= 145 nm.

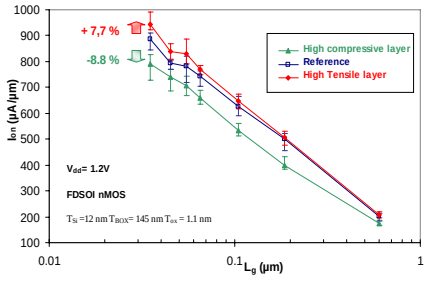


Figure 10: Impact of strained CESL on nMOS saturation current as a function of L_g.

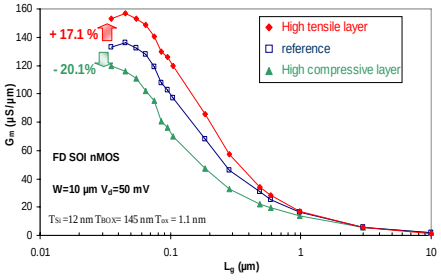


Figure 11: Impact of strained CESL on nMOS linear g_m (L_g).

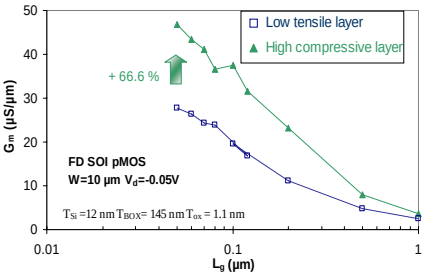


Figure 12: Impact of strained CESL on pMOS linear g_m (L_g).

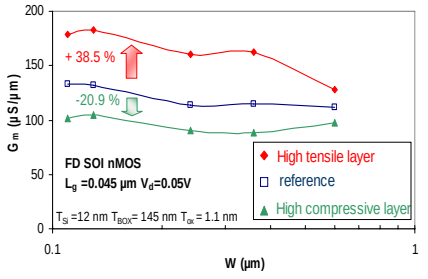


Fig 13: Impact of strained CESL on nMOS linear g_m (W).