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Performance Enhancement under High-Temperature Operation and Physical Origin of Mobility Characteristics in Ge-rich strained SiGe-on-Insulator pMOSFETs

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1. Introduction

Channel-mobility enhncement is one of key technologies for boosting performance of CMOS logic circuits. We have proposed strained Ge-rich SiGe-on-Insulator (SGOI) as high-mobility material for pMOSFETs and demonstrated the large mobility enhancement of up to 10 times at room temperature [1]. Practically, mobility enhancement at higher temperatures is more important since operating temperatures in VLSI devices are higher than room temperature. However, a normal operation and advantage in mobility at high temperatures in these devices have not been verified yet. In this work, high-temperature operation and mobility enhancement are demonstrated up to 200˚C for strained Ge-rich SGOI-pMOSFETs. Phonon-limited mobility, which ultimately dominates mobility at high temperatures, was extracted by analyzing temperature dependence of the mobility. The extracted mobility exhibited enhancement over 10 times at 200ºC, suggesting that the strained SGOI channel retains the advantage in mobility at high temperatures in operating VLSI devices.

2. Device structure

Recessed SGOI-pMOSFETs were fabricated by the local condensation technique [1]. The device had a Ge-rich channel region with compressive strain and Si-rich source/drain (S/D) regions on a buried oxide layer, in order to realize large mobility enhancement and low junction leakage current (Fig. 1). Typical device parameters were listed in Table 1 as well as calculated band gap energy, E_g [3]. Values of strain, ε, and Ge fraction, x, were determined from the Raman measurement [2]. Cross sectional TEM images in Fig. 2 showed dislocations around the S/D regions and surface undulation on the channel in the thicker device with SGOI thickness of ~25 nm, whereas showed no dislocations and a smooth oxide interface in the thinner device with SGOI thickness of ~5 nm. Correspondingly, it was found from the Raman measurements that the thicker device was partially relaxed and the thinner one was fully strained. This can be explained that the SGOI thicknesses were significantly larger than and comparable to the equilibrium critical thickness values for the thicker and thinner devices, respectively.

3. Electrical characterization

Transistor characteristics: Significant enhancement (~6 times) of saturation drain current, which was comparable to the enhancement at 27˚C, was obtained at 200˚C for the strained SGOI-pMOSFET (x=0.92) (Fig. 3). The thicker and thinner devices cut off even at 200ºC (Fig. 4), irrespective of their small E_g values for the strained SGOI channels, thanks to the lower drain leakage due to larger E_g values in the S/D regions than in the channels.

Mobility-limiting mechanisms: The dependence of mobility on temperature, T, was investigated to clarify the mobility-limiting mechanism. The observed hole mobility in the thicker device (x=0.92) was almost dependent on the effective field, E_{eff}, as E_{eff}^{-1} at T ranging from 23K to 472K (Fig. 5). Assuming simple power dependences on E_{eff} for each component of the mobility such as $\mu_{phonon} \propto E_{eff}^{-0.3}$, $\mu_{alloy} \propto E_{eff}^{-0.3}$ and $\mu_{SR} \propto E_{eff}^{-1}$ [4,5], it is suggested that the surface roughness scattering is a dominant scattering mechanism. Here, μ_{phonon}, μ_{alloy} and μ_{SR} are mobility components limited by phonon scattering, alloy scattering and surface roughness scattering, respectively. This is consistent with the TEM image indicating the rough gate-oxide interface. In the thinner device (x=0.59), on the other hand, the dependencies were between E_{eff}^{-1} and $E_{eff}^{-0.3}$, suggesting that all the three components should be considered as mobility-limiting mechanisms. The difference from the case of the thicker device is attributable to less significant surface roughness scattering due to the smoother oxide interface and more significant alloy scattering. Additional mobility degradation mechanisms due to the strong confinement and the thickness fluctuation have been reported in ultra-thin body SOI-pMOSFETs with the SOI thicknesses less than ~5 nm [6]. However, no degradation due to the thickness reduction was observed for the normalized mobility of the thinner devices by calculated enhancement factors depending on x [7] (Fig. 6).

Extraction of phonon-limited mobility: The mobility enhancement factors increased as T was increased, especially for the thicker device (Fig. 7). This was a result of the weaker temperature dependence of the mobility in the SGOI channel than in Si channel (Fig. 8), presumably due to the significant surface roughness scattering. In order to examine advantage in mobility at high temperatures for ideal strained SGOI devices with negligible alloy scattering (x~1) and moderate surface roughness scattering expected for a smooth interface, values of μ_{phonon} were extracted assuming that μ_{alloy} and μ_{SR} are independent of T and $1/\mu_{phonon}(T) = 1/\mu_{total}(T) - 1/\mu_{total}(23K)$, where $1/\mu_{total}(23K) = 1/\mu_{alloy} + 1/\mu_{SR}$. The assumptions may be reasonable since μ_{total} was almost saturated at low temperatures (Fig. 8). The extracted μ_{phonon} (T) exhibited larger values for higher x, and temperature dependences were consistent with Si-MOSFETs [4] such as $\mu_{phonon}(T) \propto T^{-1.75}$ at T>200K (Fig. 9). The obtained enhancement factors of μ_{phonon} was estimated to be 12 and 5.5 at 200˚C for the thicker (x=0.92) and the thinner (x=0.59) devices, respectively. This result indicates that significantly large mobility enhancement can be expected essentially in Ge-rich and ultra-thin SGOI-pMOSFETs.

4. Conclusion

Significantly large I_{on} enhancement was observed at T up to 200˚C in Ge-rich and ultra-thin strained SGOI-pMOSFETs. It was shown that thickness reduction of the SGOI layer, which is necessary for the CMOS scaling, allowed dislocation-free channel layer with smooth interfaces without mobility degradation. Extracted phonon-limited mobility also exhibited large enhancement factors over 5 even at T=200˚C. In conclusion, mobility advantage in ultra-thin SGOI-pMOSFETs was confirmed at temperatures comparable with or higher than operating temperatures in VLSI devices.

Acknowledgements: This work was supported by NEDO.

References

[1] T. Tezuka et al., Symp. VLSI Tech., p198, (2004). [2] J. C. Tsang et al., J. Appl. Phys. **75**, 8098 (1994). [3] M. V. Fischetti and S. E. Laux, J. Appl. Phys. **80**, 2234 (1996). [4] S. Takagi et al., IEEE Trans. Electron Devices **41**, 2357 (1994). [5] G. Höck et al., Appl. Phys. Lett. **76**, 3920 (2000). [6] K. Uchida et al., IEDM Tech. Dig. (2002). [7] F. M. Bufler and B. Meinerzhagen, J. Appl. Phys. **84**, 5597 (1998).

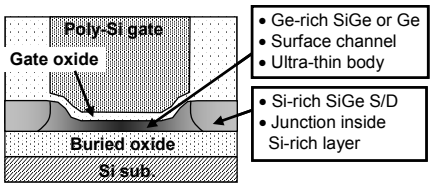

Fig. 1 Schematic diagram of fabricated device structure consisting of Ge-rich strained SGOI channel and Si-rich S/D regions.

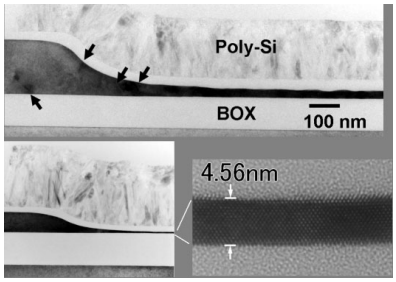

Fig. 2 Cross-sectional TEM images around S/D region for two kinds of devices with thick (~25 nm) and thin (~5 nm) channels. Arrows indicate dislocations.

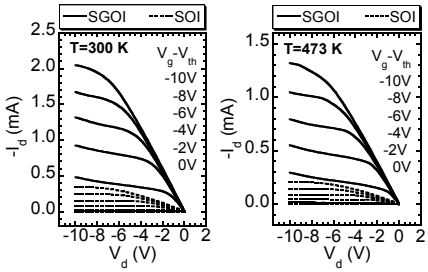

Fig. 3 Drain current as a function of drain voltage for SGOI-pMOSFET (x=0.92, ε=-1.4%) and control SOI-pMOSFET of L_g/W=200μm/100μm at room temperature (left) and at 200˚C (right). Saturation current in the SGOI-MOSFET was almost 6 times larger than in the control SOI-MOSFET at both temperatures.

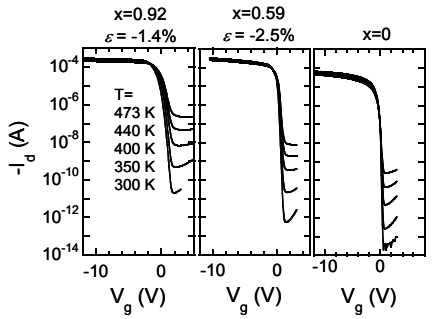

Fig. 4 Transfer characteristics for SGOI- and SOI-pMOSFETs of L_g/W=200μm/100μm at temperatures above 300K. Drain voltage, V_d, was -1 V for all devices.

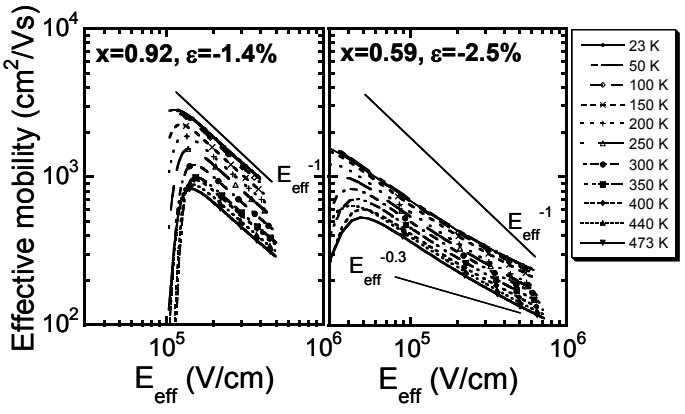

Fig. 5 Temperature dependences of SGOI-pMOSFETs as a function of effective field obtained by split C-V measurements.

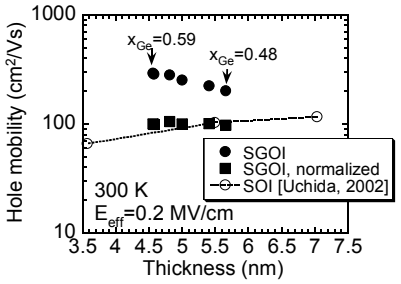

Fig. 6 Hole mobility for thin SGOI devices (●), and normalized mobility by calculated enhancement factors [7] for canceling effect of difference in x (■), as a function of SGOI thickness, which is inversely proportional to x. Published data for ultra-thin body SOI-MOSFETs [6] were also indicated (○).

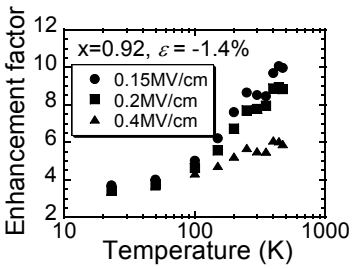

Fig. 7 Temperature dependence of mobility enhancement factor for SGOI-pMOSFETs against control SOI-pMOSFET. Enhancement factors were monotonously increased with increasing temperature.

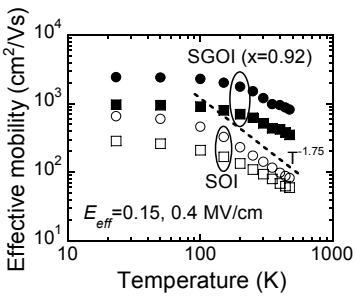

Fig. 8 Mobility dependence on temperature at fixed E_{eff} for SGOI (x=0.92)- and SOI-pMOSFETs. Mobilities were almost constant at low temperatures, while monotonously decreased with increasing temperature for both devices.

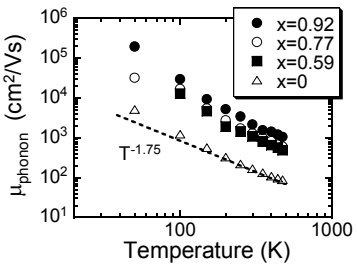

Fig. 9 Extracted phonon-limited mobility as function of temperature for SGOI- and SOI-pMOSFETs. The temperature dependencies were described as $T^{-1.75}$, which is consistent with a result for a Si-MOSFET.

S/D				channel				t_{GOX} (nm)
x	strain (%)	E_g (eV)	t_{SGOI} (nm)	x	strain (%)	E_g (eV)	t_{SGOI} (nm)	
0	0	1.15	81	0	0	1.15	31	21
0.04	-0.2	1.12	63	0.59	-2.5	0.61	4.6	20
0.12	-0.5	1.05	190	0.92	-1.4	0.73	25	37

Table 1 Major specifications of typical SGOI- and control SOI-pMOSFETs. Band gap energies, E_g, for strained SiGe were obtained by linear interpolation from [3].