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Impact of Body Bias Controlling in Partially Depleted SOI Devices with Hybrid Trench Isolation Technology

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1. Introduction

Beyond the MPU's, a silicon-on-insulator (SOI) device is extending the application to the low-power system on a chip (SOC) embedding high-frequency analog and digital circuits. However, suppression of leakage current and fluctuation of threshold voltage is becoming difficult for large scale digital and RF/analog circuits and low power memory devices. A body-tied SOI structure, which can be realized stable operation without floating body effect, is effective for SOC application [1]-[3]. In this paper, Actively Body-bias Controlled (ABC) SOI devices with a hybrid trench isolated body-tied structure is proposed for low-power SOC. Wide-range Vth controlling due to forward and reverse bias without fully depleted mode limitation enables increasing drive current and suppressing standby current. Moreover, the forward bias realized small Vth fluctuation owing to roll-off suppression. We also show that the ABC SOI technology is effective for low-voltage operation of SRAM.

2. Device Structure

Fig.1 shows the ABC SOI MOSFETs with the hybrid (partial and full) trench isolation. The SOI layer under the partial trench isolation, which surrounds source-drain (S/D) region in conventional ABC SOI MOSFETs [1], is remained only at regions from body contact to the body under the channel. The peripheral parasitic junction capacitance of the S/D region is eliminated with the full trench isolation in the ABC SOI MOSFETs. A body contact is fabricated through the partial trench isolated oxide to SOI layer and also serves as a shared contact for gate-to-body connection.

3. Features of Body Bias Controlling

In the ABC SOI MOSFET, a body bias can be controlled without area penalty and parasitic capacitance increase, contrary to H-shaped and T-shaped gate SOI MOSFETs. Fig. 2 shows Id-Vg characteristics of the ABC SOI MOSFET at 100 °C. In spite of worst temperature condition, Vth and Ioff can be controlled for high-speed or low-leakage mode by applying forward or reverse body bias. Thin SOI layer reduces junction capacitance and is effective in digital circuit. However, a very thin SOI layer is not suitable for ABC MOSFET. Fig. 3 shows a dependence of the Ioff on SOI thickness at 100 °C. In the case of thin body MOSFET, the Ioff control is limited because of full depletion in the body by applying reverse bias, but thicker body MOSFET enables to control for wide range.

Moreover, in the ABC SOI MOSFET, applying forward bias can suppress Vth roll-off characteristics as shown in Fig. 4. Forward bias can suppress the Vth fluctuation because of a narrow depletion. The Vth fluctuation is the critical issue for SRAM scaling, especially in low voltage operation.

The forward bias also can improve matching properties in pair-transistors for analog devices. Fig. 5 shows the Vth and Id fluctuations (Pelgrom plot [4]) of the ABC SOI MOSFETs. The matching property was evaluated in neighboring MOSFETs as shown in Fig. 5 (a). Fig 5 (b) and (c) show measured the Vth and Id fluctuations of the ABC SOI NMOSFETs as a function of device area (LW). In the case of applying negative body bias (Vb=-0.3V), the Vth fluctuation becomes large. However, the Vth fluctuation of MOSFETs are small at Vb=0.3V. One of the origins of the Vth fluctuation is impurity charge variation in the depletion regions under the channel. Therefore, at a forward bias condition, the depletion depth becomes a shallow, and influence of charge variation can be suppressed. Drain current fluctuation at Vb=0.3V is also small compared to that at Vb=0 and -0.3V. This is due to lowering the Vth at forward bias as well as the low Vth fluctuation. Drain current of the MOSFET increase at forward bias condition because of a large over drive (Vg-Vth), therefore ΔId/Id becomes small. From theses results, the stable operation is expected in ABC SOI SRAM at low supply voltage due to the low Vth fluctuation.

4. ABC SOI SRAM

Fig. 6 shows a schematic diagram of a cell layout for the ABC SOI SRAM. The full trench isolation is fabricated in between NMOS and PMOS, and the partial trench isolation is fabricated in well region for body contact. Direct body contact as the shared contact structure connects the word line with gate and body of access transistor and body of driver transistor. An additional area to form the gate-to-body-connection is not needed for this cell layout. Although low-Vth operation at low supply voltage induces the increases of the standby current, in this structure, the standby current does not increase at all because the body is not biased when the word line is low level.

A fail bit count is compared depending on supply voltage for the ABC SRAM with the hybrid trench isolation and the normal SOI SRAM with the partial trench isolation as shown in Fig.7. The fail bit count increased with decreasing of supply voltage in normal SRAM. This is due to a fluctuation of pair-transistors in cells. However, the fail bits are not appeared until operation error of the peripheral circuits at a supply voltage of 0.78V in the ABC SRAM. About 0.1V improvement realized for low voltage operation by utilizing the ABC technology. This technology solves the scaling obstacle of SRAM in low voltage operation.

5. Conclusion

The body bias controlling of the SOI MOSFET with the hybrid trench isolation technology was demonstrated. By using the technology, it is possible to realize low-power and high-performance circuits on SOC in 65 nm nodes and beyond.

References

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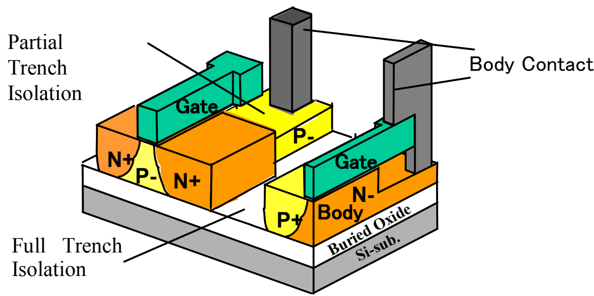

Fig. 1 Schematic diagram of ABC MOSFET. Body-tied silicon layer is located only at the side of the MOSFET.

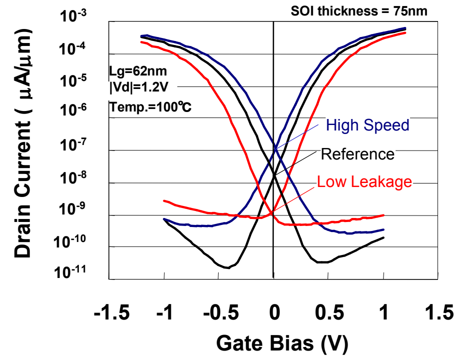

Fig. 2 Id-Vg characteristics of the ABC SOI MOSFETs at 100°C.

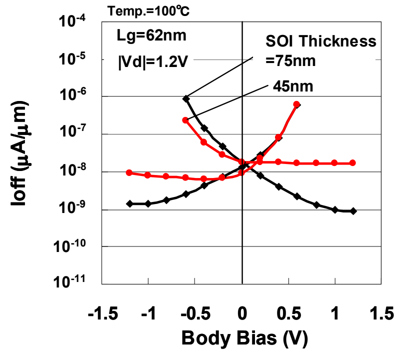

Fig. 3 Body bias dependence of Ioff in the ABC SOI MOSFETs at 100°C.

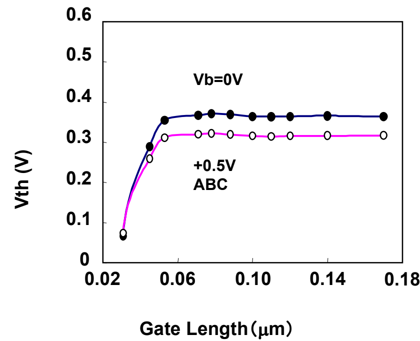

Fig. 4 Measured Vth roll-off characteristics of the ABC SOI MOSFETs. Vth roll-off is suppressed by applying forward bias.

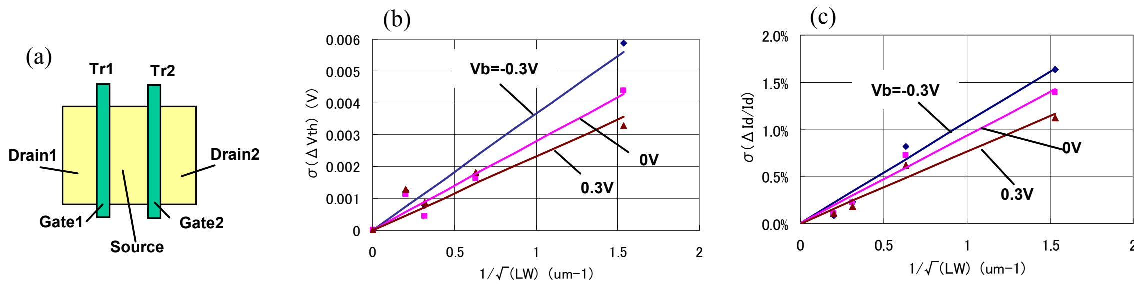

Fig. 5 Measured Vth and Id fluctuations of the ABC SOI MOSFETs. (a) schematic plane view of measured pair-transistors., (b) standard deviation of ΔVth of NMOSFETs as a function of device area (LW) for body bias of –0.3, 0, 0.3V, (c) standard deviation of ΔId/Id of NMOSFETs.

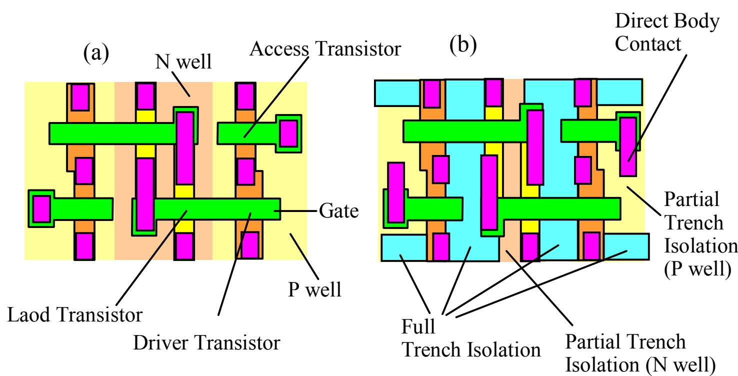

Fig. 6 Cell layout for (a) normal SRAM and (b) ABC SRAM with direct body contacts.

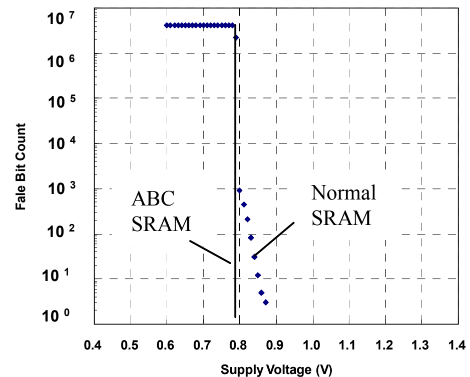

Fig. 7 Fail bit count for the normal SRAM and the ABC SRAM.