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A High Gain (25%) Strained Silicon Scheme for 65nm High Performance nMOSFETs

T Y Chang, J W Pan, Y C Liu, P W Liu, B C Lan, C H Tsai, T F Chen, C H Tung, C T Huang, C T Tsai, and W T Shiau

United Microelectronics Corporation (UMC), Central R&D Division, No. 3, Li-Hsin Rd. II, Hsin-Chu City, Taiwan 30077 (w_t_shiau@umc.com)

1. Abstract

A high gain strained silicon scheme that employs a standard CVD silicon nitride film (<0.1GPa), accompanied with a thermal treatment, on a polysilicon gate is presented. Although the maximum stress in channel region was only about 0.2Gpa, a 25% drive current enhancement of nMOSFETs has been successfully demonstrated at Lg=40nm. This is the highest drive current gain reported to date for the polysilicon strained silicon scheme. Additionally, short channel effect can be effectively suppressed due to a strain induced band offset near source and drain (S/D) region. This polysilicon strain scheme also exhibited comparable reliability characteristics to conventional nMOSFETs. Moreover, additional pre-amorphorization implantation (PAI) showed no further improvement on current gain.

2. Introduction

Many strained Si techniques that enhance current drive capability by increasing carrier mobility are reported to overcome device-scaling barriers [1,2]. Substrate strained Si technology introduces biaxial strain to improve carrier mobility by a Si/SiGe lattice mismatch [3]. However, there are a few manufacturing challenges to this method, such as wafer cost, scalability (e.g. film thickness, Ge content) and defects. Meanwhile, mechanical stress resulting from additional process steps provides another means to enhance device performance [4,5].

In this paper, we depict a current drive enhancement scheme by using a polysilicon electrode induced channel stress and optimizing drain engineering without any additional pre-amorphorization implantation (PAI) processes.

3. Device Preparation

High performance nMOSFETs were fabricated with 14A oxynitride gate dielectrics. After gate patterning, the transistors were integrated with shallow extension and pocket implants, followed by sidewall spacer formation. After S/D implantation, a standard CVD silicon nitride film (<0.1GPa) was deposited to serve as a stress source, followed by a subsequent thermal treatment for dopant activation and strain memorization. Different pre-amorphorization implantation was also applied on poly silicon gate to study the effect of PAI on strain transfer or memorization into the channel region. **Fig. 1** shows the TEM image of a 40nm stressed poly nMOSFETs.

4. Results and Discussion

A polysilicon strain scheme capping a standard low temperature tensile nitride film (<0.1GPa) to improve device performance of nMOSFETs is presented in this paper. This process scheme is compatible with standard IC industry processes without any additional lithography step. **Fig. 2** shows the Ion vs. Ioff universal plots of control and poly stress samples. An obvious current enhancement can be achieved by this poly silicon strain scheme with optimized drain engineering. As gate length scaled to 40nm, a 25% drive current gain has been demonstrated. As shown in **Table I**, **the 25% current gain is among the best results reported to date** for polysilicon strain scheme. It is also worth noted that only a low tensile nitride film (<0.1Gpa) was used for the capping layer, and no further PAI processes are required. **Fig. 3** illustrates the drive current enhancement as a function of the gate length. Channel stress significantly increases with decreasing channel length. This results in higher drive current gain at shorter channel length. This is due to the fact that polysilicon strain is localized near the S/D channel region. TCAD simulation results of strain in channel direction are shown in Fig. 4. The maximal stress is located at the interface of S/D and channel irrespective of as-deposited or final films. The simulation results demonstrate that drive current gain is a function of gate length. It also points out that although the final stress in channel region is about 0.2 GPa, an obvious current gain can still be archived. Besides the enhanced tensile stress in the channel direction, the high current gain may also be due to higher compressive stress in the out-of-plane direction. The threshold voltage roll-off characteristics of nMOSFETs are shown in **Fig. 5.** The result indicates that further modification of drain engineering is required to optimize the polysilicon strain scheme. **Fig. 6** shows drain current vs. gate voltage characteristics of control and poly stress samples. Device parameters, such as drain induced barrier lowering (DIBL) and subthreshold slope, can be significantly improved by this polysilicon strain scheme. The suppression in DIBL and improvement in subthreshold swing may be due to the strain induced band offset near S/D region. Therefore, this polysilicon strain scheme can improve not only drive currents but also SCE as devices scaled down.

Interface states were determined by charge pumping method as shown in **Fig. 7**. Corresponding behavior of interface trap states generation can be observed after stressing the ultra-thin oxide under a constant gate voltage. It is noted that the polysilicon strain scheme has no adverse effect on interface states. **Fig. 8** shows the hot carrier lifetime extraction of control and stressed samples. No significant difference in hot carrier lifetime between these two samples. Comparable flicker noise characteristics are shown in **Fig. 9**. There is no drawback of noise characteristics on this polysilicon strain scheme. In summary, interface quality, reliability and noise characteristics of the polysilicon strain scheme are comparable to that of the control sample. This current enhancement scheme would not introduce other side effects on device performance. Furthermore, the role of additional PAI on device performance has been further investigated, as described in **Fig. 10**. The devices with additional PAI process does not show higher drive current gain. Therefore, this PAI process is not an indispensable step for this polysilicon strain scheme.

5. Conclusions

A polysilicon strain scheme has been reported by using a standard low temperature nitride film and subsequent thermal activation. This scheme will induce higher tensile stress at S/D and channel regions, and then improve device characteristics including current gain and short channel effect. As gate length scaled to 40nm, a record 25% drive current enhancement of nMOSFETs is achieved with superior DIBL and sub-threshold swing. Device reliability is also comparable to control ones. Concluding, this polysilicon strain scheme will be promising for sub-65 nm high performance nMOSFETs application.

References

[1] S. Pidin, et al., pp. 213, IEDM, 2004, [2] K. Mistry, et al., pp. 50, VLSI, 2004, [3] J. R. Hwang, et al., pp. 103, VLSI, 2003, [4] K. Ota, et al., pp. 27, IEDM, 2002, [5] C. H. Chen, et al., pp. 56, VLSI, 2004, [6] R. Khamankar, et al., pp. 162, VLSI, 2004, [7] F. Boeuf, et al., pp.425, IEDM, 2004.

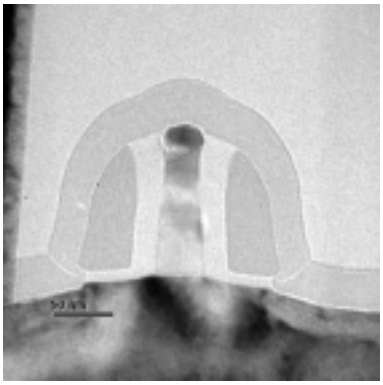

Fig. 1 TEM cross-section of a 40nm gate length nMOSFETs.

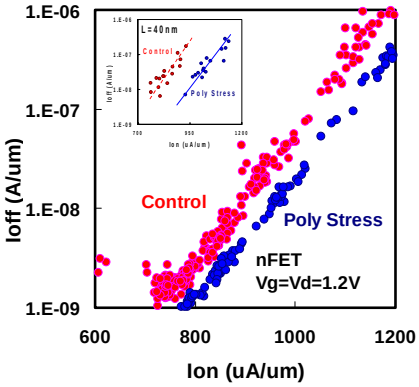

Fig. 2 Ion vs. Ioff relationship at Vd=1.2V of nMOSFET. The insert figure indicates Ion vs. Ioff plots at 40nm gate length.

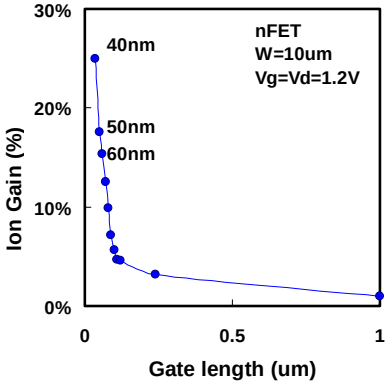

Fig. 3 On-state drive current gain vs. gate channel length relationship.

Table I Polysilicon strain scheme benchmark.

Polysilicon Strain Scheme Benchmark					
	This work	Ref [4]	Ref [5]	Ref [6]	Ref [7]
Gate length	**40nm**	55nm	65nm Node	35nm	60nm
PAI	**None**	High dose As	High dose Ge	None	Blanket Ge
Cap layer	**Low temp. SiN**	Low temp. CVD SiO_2	Low temp. SiN	CVD film	Off-set spacer
Stress (GPa)	**Tensile < 0.1**	Tensile > 0.1	Tensile > 1.5	Tensile	NA
NMOS gain	**25%**	15%	15%	10%	10%

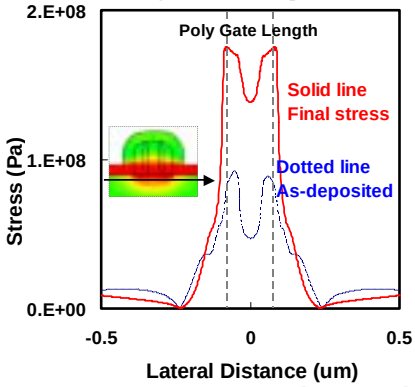

Fig. 4 TCAD strain simulation results of poly stress.

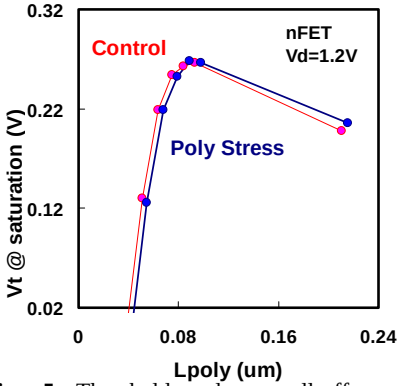

Fig. 5 Threshold voltage roll-off at saturation condition.

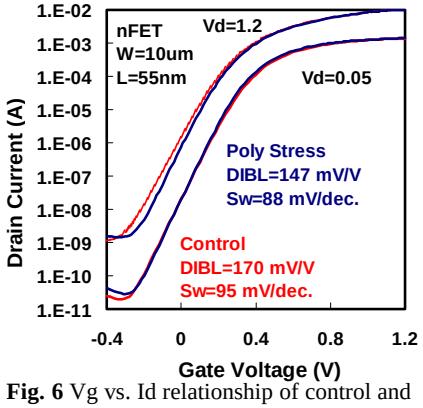

Fig. 6 Vg vs. Id relationship of control and poly stress devices.

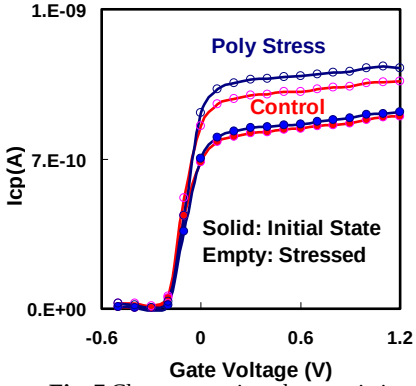

Fig. 7 Charge pumping characteristics of control and poly stress devices.

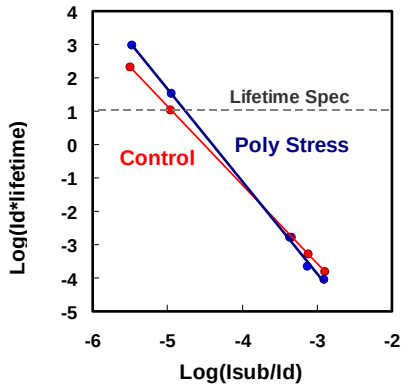

Fig. 8 HCI lifetime extraction of control and poly stress devices.

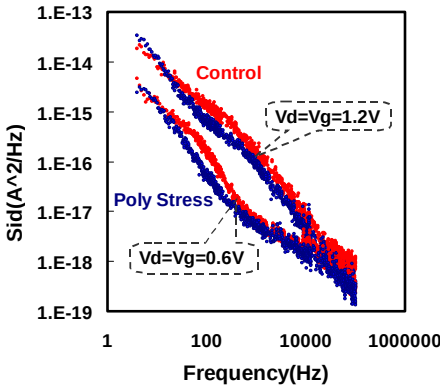

Fig. 9 Flicker noise characteristics.

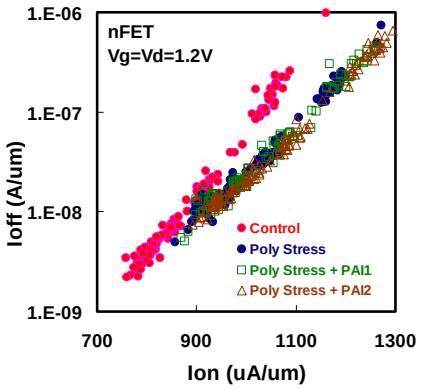

Fig. 10 Effect of pre-amorphorization implantation on poly stress scheme.