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Advanced I/O Technology using Laterally Modulated Channel MOSFET for 65-nm Node SoC

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Abstract

Advanced I/O technology has been presented for a 65-nm node SoC application, including high-speed I/O and RF circuits. Our device having laterally modulated channel shows a sufficient reliability even at a 3.3 V operation with the same size as a conventional 2.5 V device. Since this technology also improves current drivability, the layout area of an I/O circuit block can be reduced up to 55% because of a reduced total gate width. Moreover, a metal-on-gate (MOG) option has been developed for RF application, and an f_{max} of 55 GHz was achieved.

Introduction

Not only core transistor performance but also I/O technology and RF capability become very important factor for leading-edge SoC. One of the strong demands for those SoC is to handle the different power supply voltages, such as 1.8, 2.5, and 3.3 V. In addition, the number of supply voltages will increase monotonically with a technology generation progress. A transistor corresponding to each supply voltage is currently integrated in a chip by using multiple oxidation process and optimizing an impurity profile. However, this leads to higher manufacturing cost due to an increase in the number of process steps, and also leads to degradation of core transistor performance caused by multiple oxidation process. Thus, we develop an I/O transistor that can operate at a multi-power supply voltage with sufficient reliability for our 65-nm SoC technology.

Another demand for leading-edge SoC is to integrate high performance RF circuit that can operate at high supply voltage . A multi-fingered transistor layout is commonly used in the RF circuitry, such as power amplifier of wireless LAN, to minimize the gate resistance effect. However, this leads to an increase in the power consumption due to increased parasitic capacitance. This also causes a phase noise and makes a circuit design difficult. Thus, we implemented a MOG option to reduce the gate resistance for an RF application [1].

Laterally Modulated Channel MOS

In order to operate at multiple supply voltages, it is necessary to suppress both the hot carrier (HC) degradation and short channel effect at the same time. The key design concept to realize above is a laterally modulated channel, which means that the impurity concentration gradually changes in the channel from the source side to drain side (Fig. 1). Asymmetric halo implantation technique is used to obtain laterally modulated channel profile [2, 3]. By adjusting the channel dose and source side halo dose independently, short channel effect immunity and substrate current reduction can be realized simultaneously as shown in figure 2. In other words, a channel impurity concentration at the drain side can be reduced by using a source side halo when designing the transistor to be the same Vt at an Lg of 250 nm (Fig. 3). Thus, lateral electric field at the drain edge becomes small for a laterally modulated channel MOSFET (Fig. 4). Because an impact ionization phenomenon is strongly dependent on the drain electric field, HC lifetime can be extended for a laterally modulated channel. By reducing the channel concentration to 1/4 of the conventional one, the maximum substrate current can be reduced to below 1/4 at an Ion of 600 μA/μm (Fig. 5). This corresponds to the HC lifetime elongation of two orders of magnitude. Consequently, a laterally modulated channel transistor designed for 2.5 V endures 10 years operation even at the 3.3 V (Fig. 6).

The gate dielectric is also important for both reliability and current drivability. Figure 7 shows a supply voltage dependence of TDDB lifetime for 5.0-nm and 5.5-nm gate oxides. Considering a gate overdrive margin of 10% and the layout area, we determined a gate oxide thickness of 5.5 nm. Although this thickness is slightly thicker than that of the conventional 2.5 V transistor, the drive current at 2.5 V operation achieves a competitive value of 600 μA/μm by improvement of Si/SiO_2 interface roughness and optimization of the LDD condition.

By using advanced 2.5 V transistor, reduced process steps and photo masks are 16 steps and 5 masks, respectively. Since our advanced 2.5 V I/O transistor has superior HC immunity, we can operate at 3.3 V and achieves high drive current of 840 μA/μm (Fig. 8). This reduces total transistor width especially in the 3.3 V I/O block. Taking into account of the gate length scaling, we estimate that the layout area can be reduced up to 55%. Table 1 shows the summary of I/O transistor performance in this work.

MOG option

A MOG uses the metal wiring which is located above the gate, as shown in inset of figure 9. Since the metal line with low resistivity is connected with the gate through the metal contact, the input gate resistance can be lower than that of conventional silicided gate. The MOG option does not need any additional process because the gate contact and 1st metal wire in conventional process are used. Figure 9 shows the comparison of an f_{max} between cases where either the conventional gate or MOG structure is used. Device parameters are as follows ; 4-fingered NMOS, a gate length of 0.25 um, a gate width of 10 um, and a metal line width of 0.4 um for MOG. By using the MOG structure, f_{max} achieves 55 GHz which is 60% higher than that of conventional gate. From the equivalent circuit analysis, it is estimated that the effective input gate resistance is 2.2 ohm with 10 um width, which is 1/7 of the conventional silicided gate. As the result, a power gain of more than 20 dB even at 10 GHz operation can be obtained. This is a sufficient performance for designing a power amplifier of wireless communication equipments, such as wireless LAN products. Since we can design the power amplifier using high voltage transistor with MOG, a required current to achieve the target output power becomes small. Thus, narrower wire can be used to the power amplifier because the wire width is determined by the permitted current density. Therefore, we can eliminate the wiring design problem, such as phase noise and parasitic capacitance. By combining with a laterally modulated channel MOS, the output conductance can be reduced due to the smaller DIBL (Fig. 10), which leads to an improvement of a RF/Analogue circuit performance because dissipations of RF power can be suppressed.

Conclusions

We presented 65-nm CMOS technology for a SoC application focusing on the I/O transistor. By using a laterally modulated channel MOSFET, 3.3 V transistors can be replaced by advanced 2.5V transistors, which lead to reduction of transistor line-up, layout area, and hence manufacturing cost. A MOG option reduced the gate resistance and this provided a higher f_{max} of 55 GHz. We believe an I/O transistor that can be used at deferent supply voltages is indispensable for nodes of 65 nm and beyond.

References

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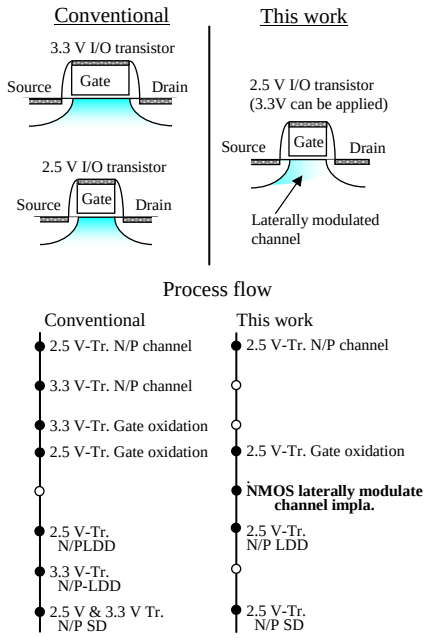

Fig. 1 Comparison between conventional process flow and this work. 5 masks (for N/P channel, N/P LDD, 3.3V oxide selective etching) and 16 process steps can be cut in this work.

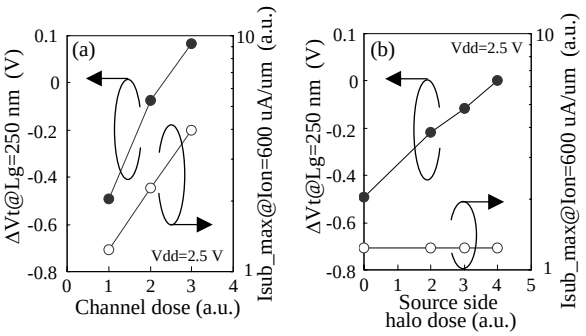

Fig. 2 ΔVt and Isub_max dependence on channel dose (a) and source halo dose (b). When channel dose decrease, both Vt and Isub_max also decrease. In contrast, Isub_max does not change when source side channel dose increases, because impact ionization occurs at drain edge.

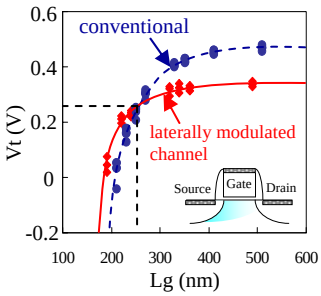

Fig. 3 Comparison of Vt-Lg rolloff curve between conventional and laterally modulated channel MOS.

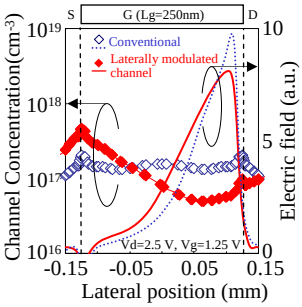

Fig. 4 Lateral profiles of the channel impurity and simulated electric field. The electric field at the drain edge becomes small for laterally modulated channel.

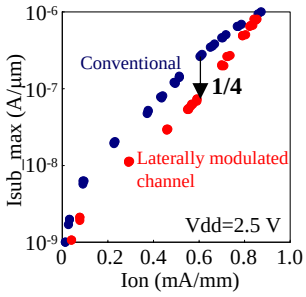

Fig. 5 Comparison of Isub_max as functions of Ion between conventional and laterally modulated channel.

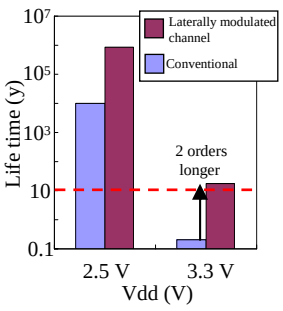

Fig. 6 Comparison of hot-carrier lifetime. By modulating the channel concentration laterally, lifetime is longer by 2 orders of magnitude.

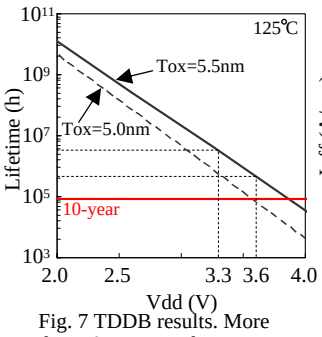

Fig. 7 TDDB results. More than 10 years can be guaranteed when 3.3 V are applied to the 5.5 nm oxide.

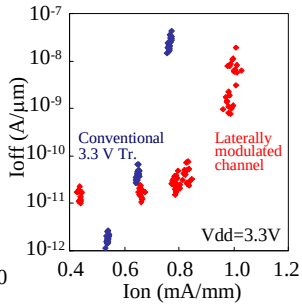

Fig. 8 Comparison of Ion between conventional and laterally modulated channel transistor.

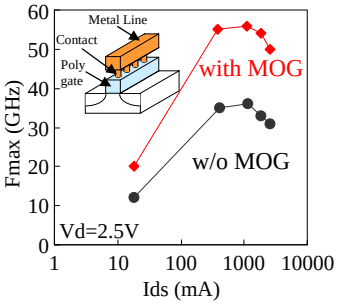

Fig. 9 Ids vs. Fmax of 4 fingered NMOS (W of a finger is 10mm). By using MOG structure, Fmax achieves 55 GHz.

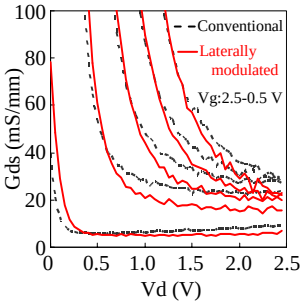

Fig. 10 Gds vs. Vd. Output conductance is improved by laterally modulated channel due to smaller DIBL.

Table 1 Summary of I/O transistor for 65nm-node SoC application.

Vdd (V)		1.8	2.5	3.3
Tox (nm)		3.0	5.5	
Gate length (nm)		180	250	
NMOS	Ion (mA/mm)	640	600	840
	Ioff (nA/mm)	0.1	0.1	0.1
PMOS	Ion (mA/mm)	310	270	420
	Ioff (nA/mm)	0.1	0.01	0.01