Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.40-41

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Direct Measurement of Circuit Performance Enhancement under Mechanically Applied Uniaxial Strain

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1. Introduction

Uniaxially/biaxially-strained silicon channel is one promising candidate for enhancing CMOS performance, and has thus been extensively investigated [1,2]. The uniaxial strain can be introduced into CMOS devices in several ways such as selective epitaxy of SiGe or SiC in the source and drain regions [2,3], applying a SiN capping layer [4], and wafer bending [5,6]. Among these, mechanically induced uniaxial strain by wafer bending is easily applicable and suitable for the investigation of carrier transport properties as well as drive-current enhancement, although its strain level is lower by one order of magnitude than that by other process induced strains.

In this paper, impact of uniaxial strain applied mechanically by four-point bending on CMOS characteristics was investigated. Moreover, enhanced circuit performance was demonstrated by direct measurement of an inverter ring oscillator under external uniaxial strain for all the combinations of channel and strain directions on a silicon (001) surface.

2. Uniaxial Stress Application

Figure 1 shows a schematic of the four-point bending method used in this work. After cutting the wafer into silicon strips containing several processed dies, they were put into the bending apparatus and tensile/compressive uniaxial stress was applied parallel/perpendicular to the channel direction. Devices having both <110> and <100> channels on a silicon (001) substrate were investigated. Surface strain of up to 0.058% (equivalent to a stress of about 94 MPa) was produced, as estimated from the equation in Fig.1. Note that positive values indicate tensile strain, and negative values compressive.

3. CMOS DC Characteristics

Figure 2 shows I_d-V_d curves of uniaxially strained FETs for long (L_g = 5 μm) and short (L_g = 50 nm) channels along the <110> direction. The direction of applied strain is parallel to the channel. It is shown that the drain currents of N- and PFETs are increased with increasing tensile and compressive strains, respectively. This strain sensitivity is much higher for the long-channel device than the short-channel one. Piezoresistance (PR) coefficients, listed in Table I [7], can be used as a good measure for predicting this drive-current enhancement as well as mobility enhancement of uniaxially-strained CMOSFETs. Figure 3 shows the uniaxial strain impact on the source/drain extension (SDE) sheet resistance (R_s). A relatively large change in PFET SDE R_s corresponds to the large PR coefficients listed in Table I, showing that the PR coefficients are still good guide in such a high impurity concentration region.

Electron and hole mobility characteristics under uniaxial strain were also evaluated, as shown in Fig.4, for the <110> channels with parallel strain direction. Unlike the case of substrate-induced biaxial strain, hole mobility enhancement is maintained even at higher effective field (> 1 MV/cm; *i.e.*, a practical operating condition), because of the additive light hole and heavy hole band splitting caused by surface confinement [8]. Figure 5 compares hole mobility under parallel strain for the <110> channel between short- and long-channel PFETs. The short-channel mobility was determined by the dR_{total}/dL_{eff} method [9], and the inversion carrier concentration for the short-channel device was estimated by the measurement of long-channel device with 2-D correction [10]. It is clear that the change in short-channel mobility is much less than that in the case of the long-channel mobility. This result is mainly due to impurity scattering induced by strong halo implants [4,11], and it agrees well with the change in I_{ds} shown in Fig.2.

4. Circuit Performance Enhancement

The impact of uniaxial strain on the circuit performance enhancement with increasing switching speed was investigated by using inverter ring oscillators (ROs) with FO = 1. Figure 6 shows the schematic layout of the inverter RO used in this work. The channels of the N- and PFETs that compose the inverter are lined up in the same direction. External uniaxial strain can therefore be applied to the N- and PFETs in the same direction at the same time.

Figure 7 shows the output waveforms of a 501-stage inverter RO under tensile/compressive uniaxial strain at a supply voltage of 1 V. It is clearly shown that compressive strain parallel to the channel and tensile strain perpendicular to the channel improve the oscillation frequency for the <110> channel, whereas tensile parallel and compressive perpendicular strains result in higher frequency for the <100> channel. The ratio of propagation delay time (τ_{pd}) as a function of applied strain is shown in Fig.8. This figure shows that τ_{pd} changes linearly with applied strain for both <110> and <100> channel directions, and the direction of their shift (slow or fast) is consistent with the I_{ds} change for each FET. τ_{pd} improvement of about 3.0% and 1.8% are obtained under 0.058% tensile strains perpendicular and parallel to the <110> and <100> channels, respectively. Further improvement in τ_{pd} is expected by using an independent channel and strain direction configuration (*e.g.*, tensile parallel strain for NFET and compressive perpendicular strain for PFET with <110> channels).

In addition to drive-current, gate and parasitic capacitances play an important role in circuit speed, and several reports have pointed out that depletion-layer capacitance is modulated with applied strain by the change in bandgap and density-of-states effective masses [12,13]. We, however, observed the negligible strain impact on the gate and junction capacitances (not shown). Figure 9 shows the relationship between τ_{pd} and the inverse of drive-current ($1/I_{dn}+1/I_{dp}$) for the <110> and <100> channel directions. The figure shows that τ_{pd} is directly proportional to the inverse of drive-current, also indicating that the capacitance change is almost negligible.

5. Conclusions

The impact of mechanically applied uniaxial strain on the CMOS circuit performance as well as DC characteristics was investigated for all the possible combinations of channel and strain directions on a silicon (001) substrate. By the direct measurement of inverter RO, it was demonstrated that the propagation delay time is improved by 3.0% under 0.058% uniaxial tensile strain perpendicular to the <110> channel mostly by drive-current enhancement.

Acknowledgement

The authors would like to thank E. Yoshida for providing the devices measured in this work. They would also like to thank Y. Kodaka for doing the wafer dicing.

References

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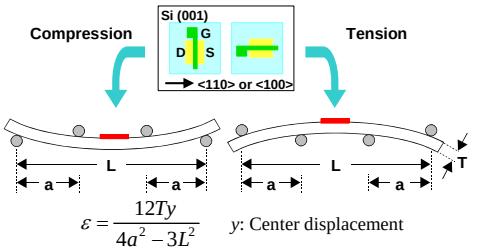

Fig.1 Schematic diagram of four-point bending method used for applying uniaxial tensile and compressive strains.

Table I First-order Piezoresistance coefficients for N- and P-type Si (001) surface [7].

Current flow direction	Stress direction		PR coefficient (x10^{-4}/MPa)	
			n-type@1e17cm^{-3}	p-type@5e17cm^{-3}
<110>	<110> (par.)	$(\pi_{11}+\pi_{12}+\pi_{44})/2$	-2.6	5.35
	<1$\bar{1}$0> (perp.)	$(\pi_{11}+\pi_{12}-\pi_{44})/2$	-1.2	-5.85
<100>	<100> (par.)	π_{11}	-7.7	-0.6
	<010> (perp.)	π_{12}	3.9	0.1

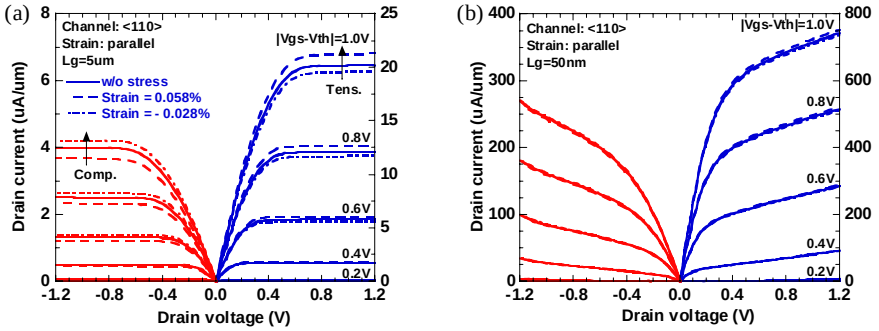

Fig.2 I_d-V_d curves of uniaxially strained FETs for gate lengths of (a) 5μm and (b) 50nm. Applied strains are -0.028% (comp.), 0%, and 0.058% (tens.) parallel to the <110> channel.

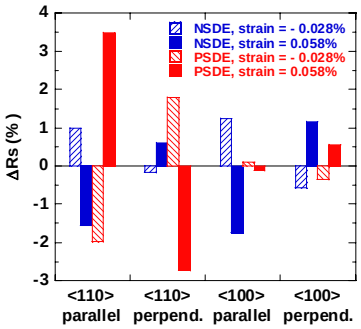

Fig.3 Uniaxial strain impact on the source/ drain extension sheet resistance.

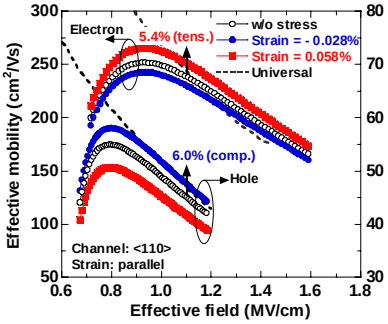

Fig.4 Electron and hole mobility under different uniaxial strain conditions.

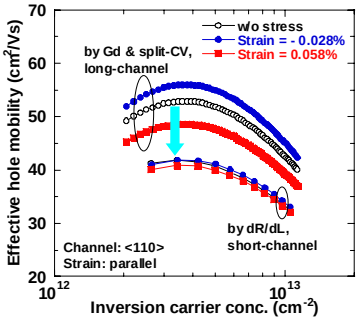

Fig.5 Hole mobility under different uniaxial strain conditions for long- and short-channel PFETs.

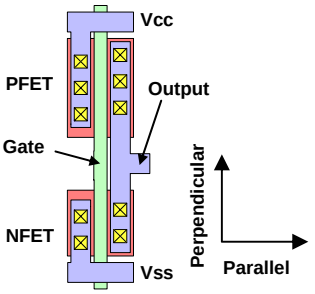

Fig.6 Schematic layout of inverter RO and the definition of applied strain direction.

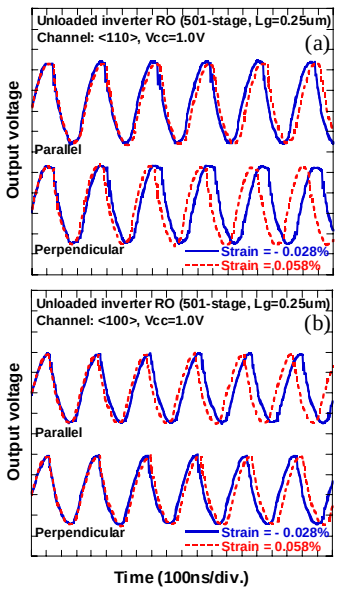

Fig.7 Output waveforms of 501-stage inverter ROs under different applied strains. The channel directions of FETs are (a) <110> and (b) <100>, respectively.

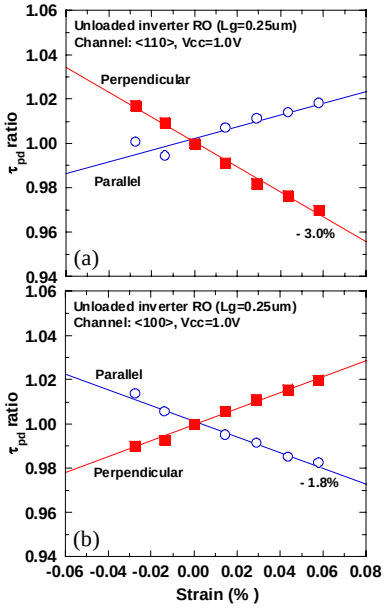

Fig.8 Dependence of propagation delay time of inverter RO on applied uniaxial strain. The channel directions of FETs are (a) <110> and (b) <100>, respectively.

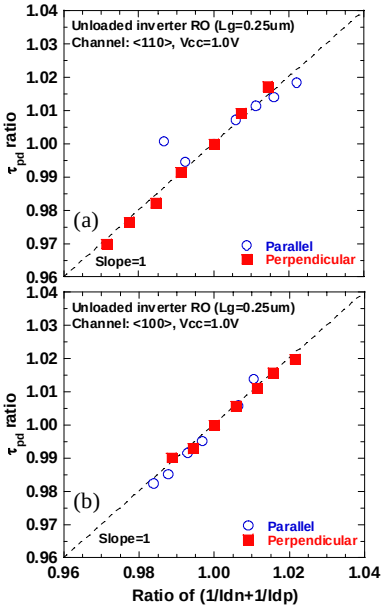

Fig.9 Relationship between propagation delay time of inverter RO and the inverse of drive-current changed by uniaxial strain for (a) <110> and (b) <100> channel directions.