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Improvement of Mobility on Ultra-thin Body SOI MOSFETs by Use of High Pressure Hydrogen Annealing

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1. Introduction

In the last few years, ultra-thin film SOI (silicon-on-insulator) technology has emerged as an attractive candidate for future IC application due to better short channel behavior, higher speed and lower power consumption.[1] But, it is reported that if the silicon film layer is thin enough, the presence of the buried oxide interface plays a very important role on mobility.[2,3] For the silicon thickness below 20nm, coulomb scattering due to interface trap sites at the back interface can degrade the mobility.[4] Performance degradation such as mobility has become serious problem as device is scaled down.

Although many mechanisms for the mobility degradation with decreasing the SOI thickness have been reported, the method of mobility enhancement has not been discussed yet. In this paper, we have investigated the improvement of mobility on UTB (Ultra-Thin Body) SOI MOSFETs by use of high pressure hydrogen annealing.

2. Device Fabrication

In this study, p-type (100) Unibond SOI wafer, produced by Smart Cut was used with the top silicon thickness of 100nm and buried oxide thickness of 200nm. Silicon thickness was decreased by etching of the sacrificial oxide layer at 1030°C by thermal oxidation. Different top silicon thickness was used on the same wafer for comparison of mobility. Isolation was achieved with MESA isolation process. The 5nm gate oxide was grown thermally at 875°C for 2min. A poly-Si layer of 100nm was formed as a gate material. After gate patterning, plasma doping was done using PH_3 at 3kV for 10min followed by rapid thermal annealing (RTA). There was no LDD and no spacer formation. Then, metallization and forming gas annealing were done. Finally, high pressure 10atm annealing in hydrogen ambient was performed for 20min at 300°C.

Mobility versus effective field was measured using SOI nMOSFET with L = 20μ m and W = 20μ m.

3. Results and Discussion

We have focused on mobility and subthreshold characteristics of thin film SOI MOSFETs. Fig. 1 shows the schematic view of device structure in this study. All samples are annealed at same high pressure condition. Typical current- voltage (I-V) characteristics of the 50nm SOI nMOSFET are shown in Fig. 2 and 3. The SOI nMOSFET which is annealed at high pressure hydrogen ambient have an excellent subthreshold swing as 65mV/dec and a high transconductance.

Fig. 4 and 5 show the E_{eff} dependence on the inversion-layer mobility. In Fig. 4, it can be seen that mobility is degraded with decreasing top silicon thickness. This is caused by the influence of buried oxide interface as top silicon thickness is scaled down. In other words, the buried oxide has great importance of mobility on SOI MOSFETs, which is caused by coulomb scattering.[4] For the mobility improvement, high pressure hydrogen anneal is introduced. Fig. 5 shows that mobility become higher after high pressure hydrogen annealing for 20min at 300°C.

To estimate the influence of oxide interface after high pressure annealing, we measured the subthreshold characteristics. The behavior of front and back channel subthreshold slope is shown in Fig. 6 (a) and (b). The high pressure effect is obvious as subthreshold swing is improved at both interfaces. As there are two oxide interfaces on SOI wafer, the effect of high pressure on SOI MOSFETs can become larger than bulk Si MOSFETs.

Fig. 7 shows the drain current versus gate voltage characteristics on ultra-thin SOI. It is also shown the subthreshold swing increase compared with forming gas annealing.

4. Conclusions

The effect of high pressure hydrogen anneal on ultra-thin body SOI MOSFETs is demonstrated. It has been found that electrical characteristics of the buried oxide layer affect the channel mobility. There are significant improvement of mobility and subthreshold swing after high pressure hydrogen annealing. It is attributed to oxide quality at both interfaces and reduced interface trap sites. Thin film SOI MOSFETs will be promising in the future and the present study will contribute the performance improvement of SOI device.

Acknowledgements

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References

[1] D. Esseni et al., IEDM Tech.Dig., (2000) 671
[2] A. Toriumi et al., IEDM Tech.Dig., (1995) 847
[3] A. Yoshino et al., Jpn.J. Appl.Phys., 37(1998) 3933
[4] J. Koga et al., IEEE Trans.Electron Device, 49 (2002) 1042
[5] H. Park et al., SSDM.,(2004) 748

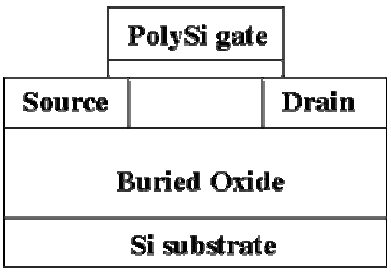


Fig. 1 Schematic of device structure

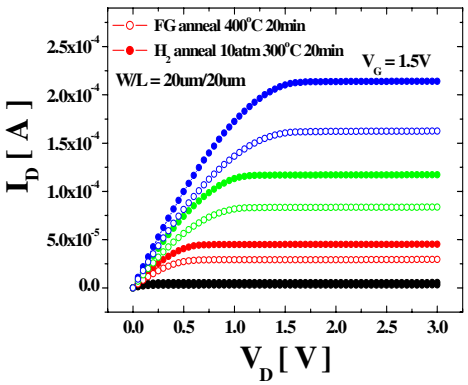


Fig. 2 Typical V_D-I_D characteristics

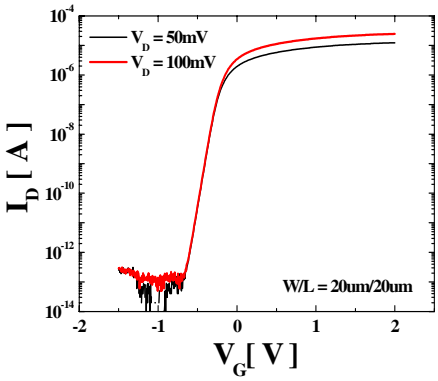


Fig. 3 (a) Drain current versus gate voltage of T_{si} = 50nm

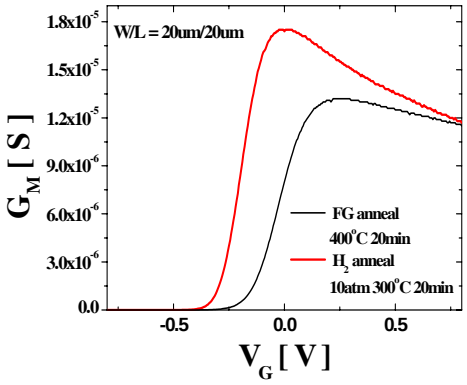


Fig. 3(b) Transconductance Versus gate voltage

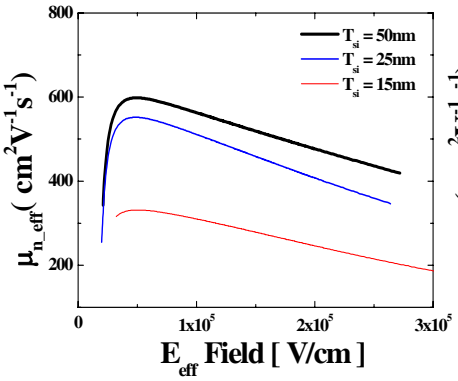


Fig. 4 E_{eff} dependence of electron mobility with different top silicon thickness.

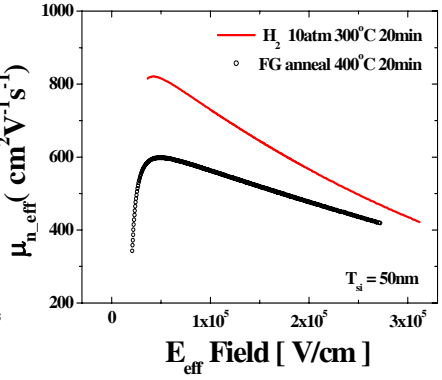
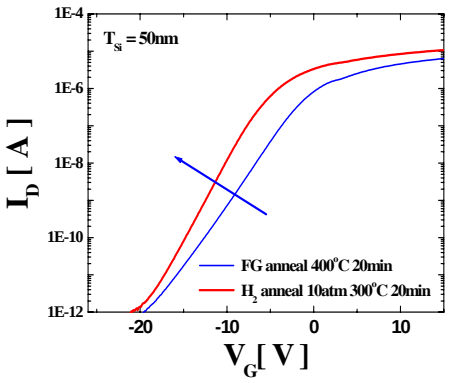
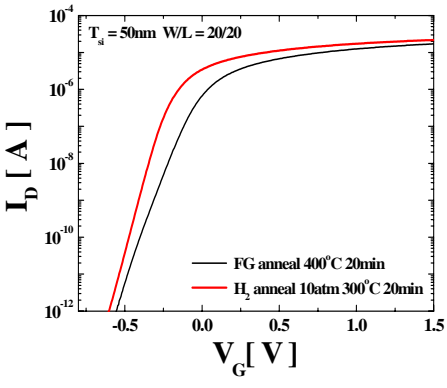


Fig. 5 The improved effective mobility on 50nm SOI.



(a)



(b)

Fig. 6 Subthreshold characteristics of 50nm SOI sample.
(a) back channel subthreshold characteristics .
(b) front channel subthreshold characteristics

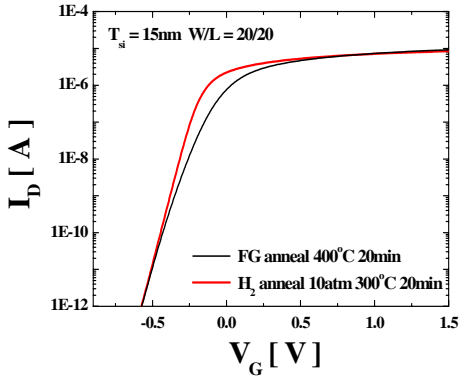


Fig. 7 Improved subthreshold slope of 15nm SOI.