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Fully-depleted ultra narrow (~10 nm) body Gate-All-Around CMOS transistors

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INTRODUCTION

Device structures such as double-gate Fin-FET, tri-gated MOSFET, Pi-gate MOSFET and Ω-shaped FET [1-5] have attracted much attention for their ability to enhance the electrostatic control of gate over the channel. Unlike planar MOSFET, the gate on these devices controls the channel from more than one-side which suppresses the short channel effects (SCE) and improves I_{on}/I_{off} ratio. Gate-all-around (GAA) ultra thin and/or narrow body transistor has gate control from all sides and therefore is a very important device structure for extreme CMOS scaling. The theoretical studies by Auth et al. [6], clearly show 40% enhancement in scaling using GAA structures in comparison to double gate transistors. However, due to process complexity, very few experimental results have been reported on such devices [7-11] with very limited device data, most of which are not exactly a combination of GAA and ultra narrow body channels.

In this work, using alternating phase shift mask lithography and self-limiting-oxidation techniques [12], we demonstrate the fabrication of n- and p-type GAA FETs on SOI with ultra narrow (~10 nm) silicon fin as the body. The devices exhibit excellent electrostatic control e.g. sub-threshold slope (SS) ~ 63 mV/dec, I_{on}/I_{off} ~10^7 and drain induced barrier lowering (DIBL) ~ 40 mV/V. We report, for the first time, that GAA devices are fully immune to the substrate bias, which makes them free of soft errors and suitable candidates for radiation hardened devices. We also demonstrate that the multi-fin GAA scales up the drive current in proportion to the number of fins without loosing much on electrostatic control and therefore can be used for high performance applications.

FABRICATION

Fig. 1 shows the process flow of MOSFET fabrication. 200 mm (100) SOI wafer is the starting material with top Si-thickness of 200 nm on 150 nm buried oxide (BOX). The active areas were patterned and etched down to the BOX to make 100 to 500 nm long Si-fins with critical dimension (CD) ~70 nm between source and drain using alt-PSM lithography and dry etching processes. The patterned Si was then oxidized in dry O_2 at 875ºC for 5 hrs. As oxide grows by consuming Si from the 3 directions of the fins, stress builds up on Si which retards the oxidation progressively and results in ultra narrow Si fins of width ~10 nm. The fins were released from oxide using wet etch process. Fig.2 shows the fully released single and multiple ultra narrow hanging fins. The central bright region is so thin that it is almost transparent to the imaging electrons under SEM. The fin release was followed by 10 nm gate dielectric and 130 nm amorphous silicon (α-Si) depositions. After S/D implant, a longer annealing was used to allow the dopants to diffuse uniformly in the α-Si gate surrounding the fin. The TEM crossection of a 100 nm long, 100 nm tall and 10 nm thick fin fully wrapped by gate oxide and α-Si is shown in Fig. 3.

RESULTS AND DISCUSSION

Fig. 4 shows the I-V characteristics of the GAA transistors with 10 nm thick, 100 nm tall and 100 nm long Si-fin as the body. The n-FET shows almost DIBL free (~10 mV/V) I_d-V_g characteristic with close to ideal sub-threshold slope (~66 mV/dec). The p-FET shows poorer DIBL (~40 mV/V) with a sub-threshold slope of 76 mV/dec, which could be a result of longer implant activation. Considering the volume inversion in the channel body (current normalized to the height of the fin [13]), the drive current of 950 μA/μm and 510 μA/μm are obtained for n-FET and p-FET respectively with off-state current in sub-nA regime. On these devices, good electrostatic control of gate on channel despite the use of 10 nm thick gate oxide indicates that the body thickness and GAA feature plays a more dominant role than the gate oxide scaling. For instance, a planar p-FET fabricated together with GAA on the same wafer gives worse sub-threshold (250 mV/dec).

Fig. 5 shows the effect of channel body length on I_{on}/I_{off} for n- and p-FET respectively. There is a little decrease (~10^7 to ~10^6) in I_{on}/I_{off} with an increase in fin length from 100 to 200 nm due to reduction in drive current with an increase in channel length. We did not observe any change in off-state current across the fin length, which indicate that SCEs are fully controlled down to 100 nm fin length.

Fig. 6 shows substrate bias effect on the threshold voltage for 100 nm long, 100 nm tall and 10 nm thick Si-fin GAA n- and p-FETs and corresponding control devices which are planer SOI MOSFETs. As obvious from the figure, there is absolutely no change in the threshold for GAA n- and p-FETs with the applied substrate bias from -5 to 5V (not shown but no change was found from -20 to 20V). In contrast, V_{th} of the control n- and p-FETs changed significantly as expected. The immunity of GAA devices to substrate bias is a result of shielding of the transistor body by the gate electrode which also indirectly verifies that poly Si below the channel body is conducting well i.e. the implanted dopants in poly have reached below the fins. The substrate bias independence of these transistors makes them very suitable candidates as a soft error immune and radiation hardened devices where any generation or recombination of electron-hole pair in the substrate can not make the device to fail.

Shown in Fig. 7 are I_d-V_g and I_d-V_d characteristics of multiple channel (five-in-one) GAA n-FET where five lateral fins are used to make one transistor. The drive current is increased to almost 5X (413 μA) to that of a single fin GAA (95 μA) without loosing much on SS and DIBL. Increasing the number of fins can thus be used to increase the drive current as needed for high performance applications.

CONCLUSION

We have demonstrated a fully CMOS-compatible fabrication method for ultra narrow Si-fin GAA n- and p- FETs on SOI wafers. The alt-PSM lithography and self limiting oxidation are used to fabricate Si-fins down to 10 nm in thickness. High I_{on}/I_{off}, Low DIBL and near ideal sub-threshold slope makes the GAA devices very suitable for low power applications. Besides excellent electrical performance, these devices are found immune to substrate bias, which makes them a very suitable candidate for soft error immunity and radiation hardened devices.

REFERENCES

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FIGURES

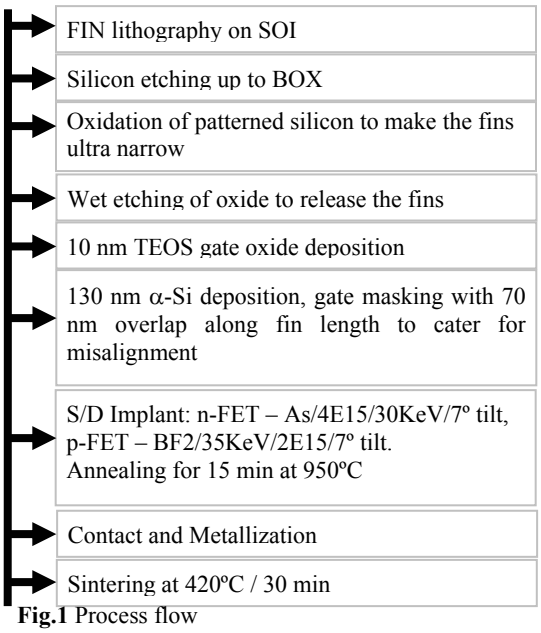


Fig.1 Process flow

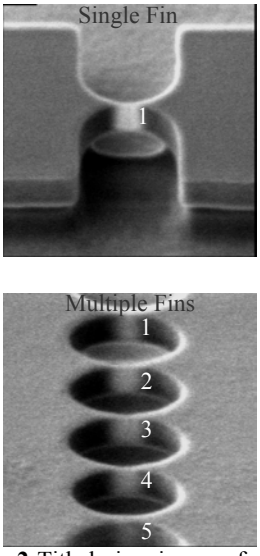


Fig. 2 Titled view image of released ultra-narrow single and multiple fins.

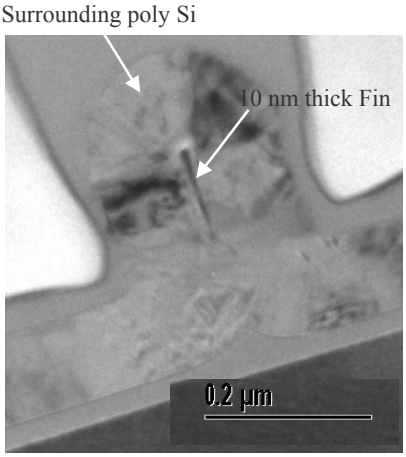


Fig. 3 TEM image of an ultra narrow (~10 nm thick), 100 nm tall silicon fin after gate α-silicon deposition. The fin is fully wrapped in side the α-Si showing a true GAA structure.

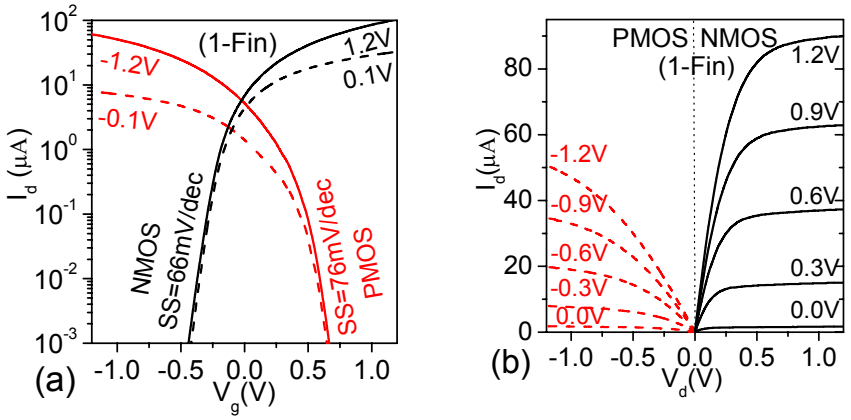


Fig. 4 I -V characteristics of ~10 nm thick, 100 nm long and 100 nm tall silicon body GAA transistors. (a) I_d-V_g plots (b) I_d-V_d plots – the number shown in volts with each curve is gate overdrive (V_g-V_{th}). For both the plots, the currents are per device.

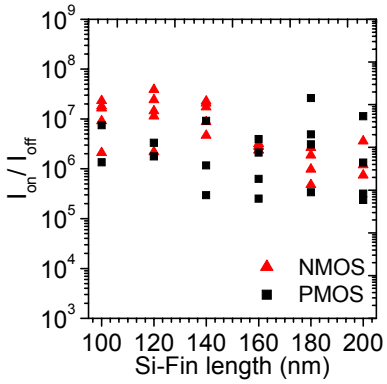


Fig. 5 Effect of fin length of GAA NMOS and PMOS transistors on I_{on}/I_{off}.

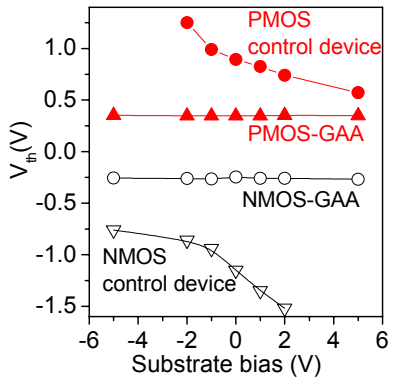
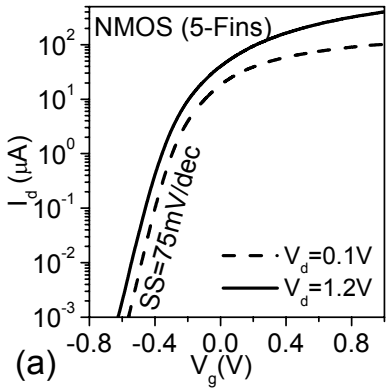


Fig. 6 Effect of substrate bias on GAA n- and p-FET devices with a comparison to control devices.



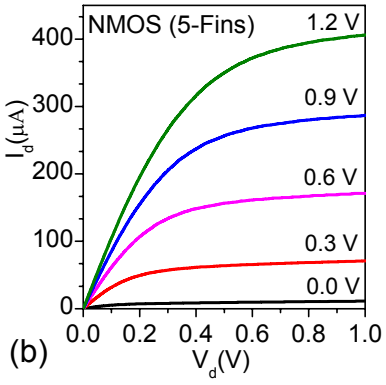


Fig. 7 I -V characteristics of five ~10 nm thick, 100 nm long and 100 nm tall lateral Si-fins GAA n-FET (a) I_d-V_g plots (b) I_d-V_d plots - the number shown in volts with each curve is gate overdrive (Vg-Vth). For both the plots, the currents are per device.