Extended Abstracts of the 2005 International Conference on Solid State Devices and Materials, Kobe, 2005, pp.260-261

B-3-2

# Si Substrate Orientation Induced Worse Hot Carrier Degradation in Novel (110)/<111'> Oriented Devices

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## ABSTRACT

High $I_{d\text{-}sat}$ enhancement of pMOSFETs with a 4-fold symmetry is benefited from novel (110)/<111'> oriented devices [1]. However, larger hot carrier degradation was observed on (110) Si substrate orientation. Furthermore, the $I_{d\text{-}sat}$ enhancement was also found to be channel length dependent. Although the impact ionization rate of oriented devices is slightly smaller than that of control devices due to larger interface scattering, higher interface bond density causes larger $N_{it}$ generation rate and makes the hot carrier degradation worse.

## INTRODUCTION

In order to integrate nMOSFETs and pMOSFETs mobility enhancements, hybrid device structures with different crystal orientations have emerged as indispensable options [2,3]. A 4-fold symmetry zones between <111> and <112> directions on (110) surface substrate, namely (100)/<111'> zone for convenience, were investigated to be one of the major approaches [1]. However, little research has been done on its reliability issues. In this paper, we investigate the drain bias, gate bias, and channel length dependence of drain current enhancement on oriented devices. In addition, the impact of hot carrier degradation on this novel oriented device was exposed for the first time. Hot carrier impact ionization of oriented devices was compared with that of control devices. The worst case of hot carrier degradation was identified. The hot carrier lifetime of both devices was extrapolated. Finally, the proper explanation of worse hot carrier degradation in (110)/<111'> orientation devices is purposed.

## DEVICE AND CHARACTERIZATION

The hole mobility of <111'> zone on (110) substrate measured with 10um devices is shown in **Fig. 1**. A 70 % mobility gain as compared with conventional devices on (100)/<110> substrate is observed, which is about 83% of the (110)/<110> mobility from reference [3]. **Fig. 2**. showed the basic electrical characteristic Id versus Vd of control devices and oriented devices. It revealed a significant current gain of pMOSFETs for oriented devices, which results from the smaller effective mass inducing mobility enhancement. However, It was shown that the drain current increment varies with drain bias. The relationship between $\Delta Id$ and Vd is shown in **Fig. 3**. At lower drain bias, the drain current is in the mobility dominant region and the $\Delta Id$ is significant since there is a large mobility difference between oriented and control devices. As the drain bias increasing, interface scattering becomes serious and causes the decrease of $\Delta Id$. Also, the $\Delta Id$ increases as well as Vg-Vt. Higher Vg-Vt induces more inversion holes and hence the interface scattering becomes less effective on drain current. **Fig. 4**. indicated that larger $\Delta Id$ is available in longer channel length. This will cause an application limit as the device dimension keeps on shrinking.

## RESULTS AND DISCUSSION

First, The impact ionization current in oriented devices was compared with that in control devices. **Fig. 5.** and **Fig. 6.** showed the impact ionization substrate current of nMOSFETs and pMOSFETs in both devices with various channel length. The difference of substrate current indicated that the impact ionization efficiency in (110)/<111'> oriented devices is smaller than that in (100)/<110> conventional devices. The impact ionization rate of both devices measured at maximum $I_{sub}$ was depicted in **Fig. 7.** It has been reported that the interface states and hydrogenated dangling bonds density of (110) orientation devices are larger than that of (100) orientation devices [4,5]. This phenomenon correlates closely with the density of surface Si atoms on different orientations. Accordingly, the small impact ionization rate in oriented devices might be due to the larger interface scattering and lattice scattering since there are more interface states and lattice atoms in channel direction. As the gate bias rises to Vg=Vd, the portion of interface scattering becomes more and more important and causes the even smaller impact ionization in oriented devices, as shown in **Fig. 8.**

The worst stress gate bias of both oriented devices and control devices would be discovered. The drain current degradation of nMOSFETs and pMOSFETs at various stress gate bias were shown in **Fig. 9.** and **Fig. 10.** respectively. All devices were stressed at equivalent stress time, 3000 sec, and stress drain bias, 2V for nMOSFETs and –2.2V for pMOSFETs. The worst stress condition of both n/pMOSFETs occurred at Vg=Vd [6], where oriented devices showed a larger drain current degradation. This result is contrary to the impact ionization substrate current shown in Fig. 8. In order to clarify the root cause of the worse hot carrier degradation in (110)/<111'> devices, the impact ionization rate versus lifetime of hot carrier stress in nMOSFETs was plotted in **Fig. 11.** Unlike the bandgap narrowing induced lifetime to $I_{sub}/Id$ slope increasing in strained Si devices [7], the oriented devices showed a parallel lifetime curve with control devices. It implies that both $\varphi i$ and $\varphi it$ are compatible in oriented and control devices [8]. **Fig. 12.** showed the PMOS hot carrier lifetime in a more general way, lifetime versus 1/Vd [9], which revealed a result similar to what was shown in NMOS.

It has been reported that the inversion carriers will affect the degradation measurement through the screening effect. Accordingly, stressed devices should be evaluated under the same inversion carrier density by keeping Vg-Vt constant [10]. Results in **Fig. 13.** demonstrated that after eliminating the influence of Vt, oriented devices still showed worse hot carrier degradation. The impact ionization depth could also affect hot carrier degradation. Thus, the impact ionization induced gate current was monitored to clarify this issue (**Fig. 14.**) [10]. The result showed no significant difference of impact ionization depth between these two devices since the Ig over Ib ratio, which represents the HC-injection efficiency, is compatible with each other. The interface state trapping density determined by the charge pumping method is shown in **Fig. 15.** It revealed that the oriented devices have a larger initial interface state density. **Fig. 16.** indicated that the NBTI lifetime of oriented devices is smaller than that of control devices due to higher interface bonds density, which could be explained as the root cause of the worse drain current degradation of hot carrier stress in oriented devices.

## CONCLUSIONS

The higher interface scattering on (110)/<111'> orientation will cause the application limit at saturation region on short channel devices. In addition, this paper revealed that although the impact ionization rate of oriented devices is slightly smaller than that of control devices due to larger interface scattering, the worse hot carrier degradation was observed in oriented devices. After eliminating all other causes, such as the differences of impact ionization rate, threshold voltage, and HC-generation depth, which may influence hot carrier degradation, this larger interface bonds density of nature was clarified to be the main cause of worse hot carrier degradation in oriented devices.

## REFERENCES

[1] J.R. Hwang, *et al., VLSI, p.90,* 2004. [2] T.Ghani, *et al., IEDM,* 2003. [3] M. Yang, *et al., IEDM,* 2003. [4] H.S. Momose, *et al., VLSI, p.77,* 2004. [5] Shigenobu Maeda, *et al., IRPS, p.8,* 2004. [6] E. Li, *et al., IRPS, p.253,* 1999. [7] M.F. Lu, *et al., IRPS, p.18,* 2004. [8] Chenming Hu, *et al., JSSC, p.295,* 1985 Feb. [9] Igor Polishchuk, *et al., IRPS, p.425,* 2001. [10] E. Murakami, *et al., VLSI, p.119,* 2001.

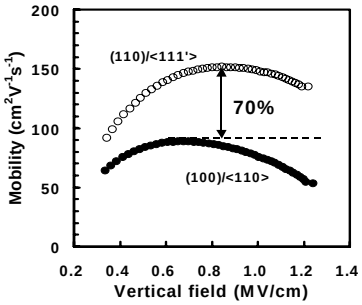


**Fig. 1** Hole mobility of control (100)/<110> devices and oriented (110)/<111'> devices.

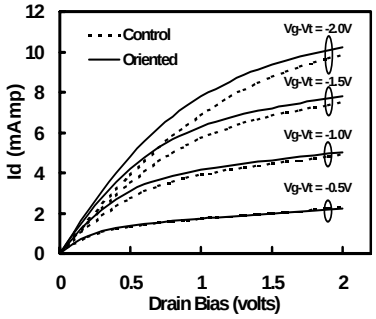


**Fig. 2** pMOSFETs Id-Vd characteristic of control and oriented devices at different gate bias with Wmask = 10μm and Lmask = 0.08μm.

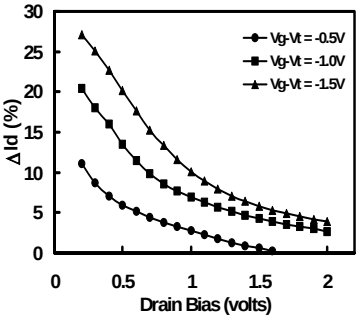


**Fig. 3** ΔId versus Vd plot at various gate bias, where ΔId = Id (oriented) – Id (control).

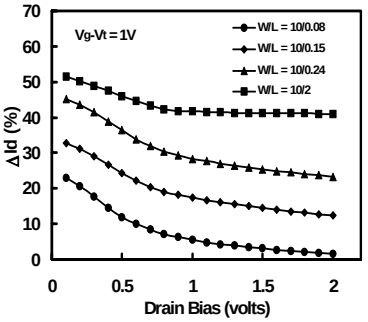


**Fig. 4** ΔId versus Vd plot at various dimensions. Lmask = 0.08, 0.15, 0.24, and 2μm respectively.

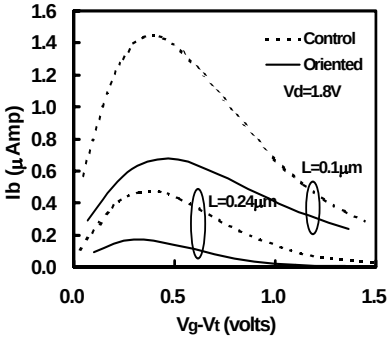


**Fig. 5** nMOSFETs impact ionization Ib versus Vg characteristic for control devices and oriented devices

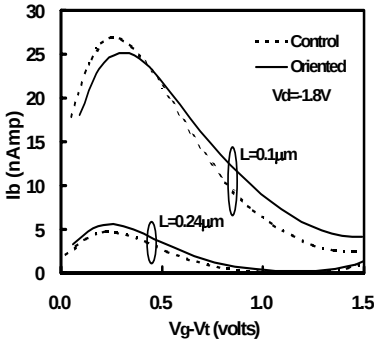


**Fig. 6** pMOSFETs impact ionization Ib versus Vg characteristic for control devices and oriented devices

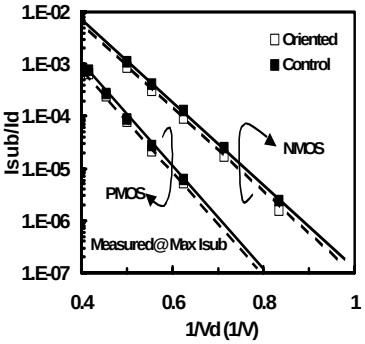


**Fig. 7** Impact ionization rate at Isub,max versus 1/Vd of both n/pMOSFETs for control devices and oriented devices.

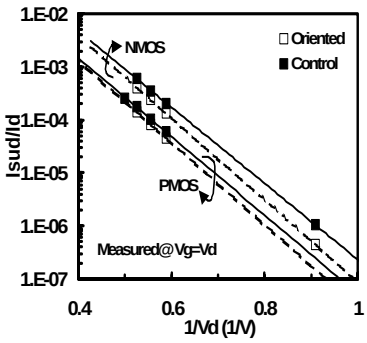


**Fig. 8** Impact ionization rate at Vg=Vd versus 1/Vd of both n/pMOSFETs for control devices and oriented devices.

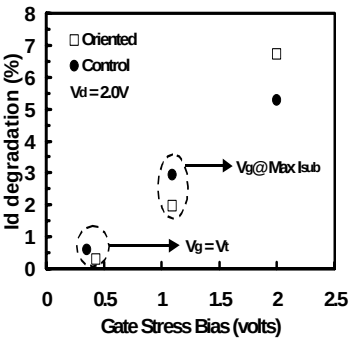


**Fig. 9** nMOSFETs drain current degradation after 3000sec stress at various stress gate bias for control and oriented devices with Wmask = 10μm and Lmask = 0.08μm.

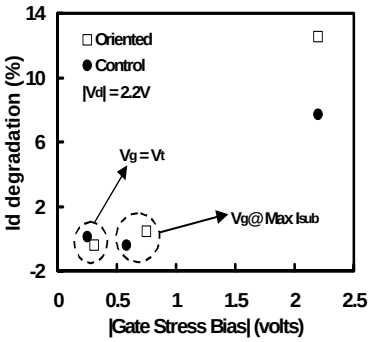


**Fig. 10** pMOSFETs drain current degradation after 3000sec stress at various stress gate bias for control and oriented devices with Wmask = 10μm and Lmask = 0.08μm.

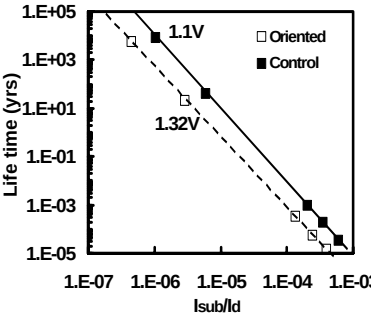


**Fig. 11** nMOSFETs HCI result of control and oriented devices. Wmask/Lmask = 10μm/0.08μm.

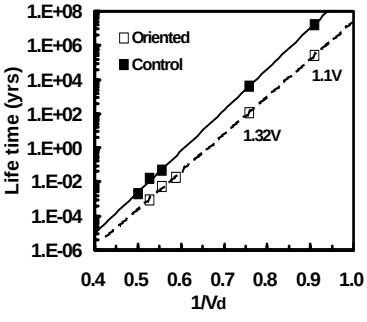


**Fig. 12** pMOSFETs HCI result of control and oriented devices. Wmask/Lmask = 10μm/0.08μm.

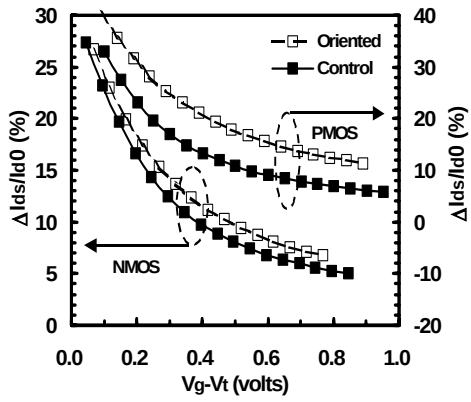


**Fig. 13** Drain current degradation rate versus Vg-Vt of both N/PMOS for control and oriented devices. Vg-Vt is a good measure to normalize the threshold voltage related device sensitivity.

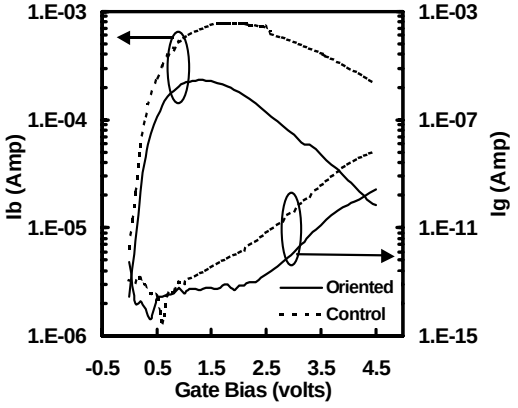


**Fig. 14** Impact ionization induced gate current in control and oriented devices with Tox = 5.2nm, Wmask = 10μm and Lmask = 0.24μm.

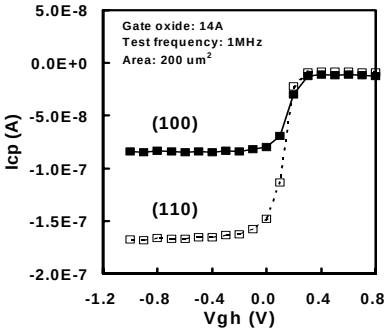


**Fig. 15** Charge pumping current of control (100) and oriented (110) devices.

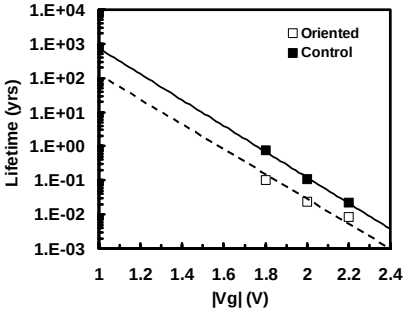


**Fig. 16** Negative Bias Temperature Instability of control and oriented devices.