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Device Design of High-Speed Source-Heterojunction-MOS-Transistors (SHOT) under 10-nm Regime

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I. Introduction

Recently, we have proposed novel high performance MOSFETs utilizing high velocity electron injection by excess kinetic energy of the conduction band offset energy ΔE_c at the source heterojunction and have actually demonstrated the transconductance (G_m) enhancement [1]. The source band offset have been experimentally realized by introducing heterostructures composed of the source region with small electron affinity, χ, and the channel region with large χ, such as the relaxed-SiGe-source/strained-Si-channel structures [1] and the relaxed-$Si_{1-x}C_x$-source/Si-channel structures [2]. In this source-heterojunction-MOS-transistor (SHOT), G_m enhancement has been found to strongly depend on the drain bias V_d [1]. Large ΔE_c induces high excess kinetic energy of electrons in SHOT. However, high parasitic resistance at the source heterojunction is caused by the high barrier height in this large ΔE_c. Therefore, it is necessary to optimize SHOT structures, especially the ΔE_c value for realizing large G_m enhancement in wide range of V_d.

In this study, using 2D device simulation, we have investigated the optimum design of SHOT structures in 10nm-region for realizing high-speed operation. In particular, we clarify optimum values of ΔE_c and the role of graded heterojunction source structures with considering scaled supply voltage.

II. Design Concept for High-Speed SHOT

As shown in the cross section of SHOT in Fig.1, the source conduction band offset is formed by the electron affinity difference between the source and the channel regions. Using the source heterojunction, high velocity electrons are injected into the channel from the source region. In order to enhance the drive current of SHOT, it is necessary to inject the high velocity electrons efficiently in wide range of V_d. Fig.2 shows the conduction band energy profile from the source to the drain regions in SHOT with linearly graded heterojunction source structures. Both ΔE_c and the length of this graded heterojunction region (L_H) are key parameters for designing SHOT in this study. Large ΔE_c leads to high velocity electron injection, but it also causes high barrier height and resulting large parasitic resistance at the heterojunction. Since this barrier height depends on V_d, it is necessary to optimize ΔE_c with considering the effect of V_d. On the other hand, L_H is also expected to affect the high velocity electron injection. Namely, long L_H induces the barrier height lowering at the source heterojunction, but the high velocity electron injection decreases with increasing L_H. Therefore, L_H is also needed to be optimized.

In order to study the influence of both ΔE_c and L_H on the drive current of SHOT in 10-nm region, we have carried out 2D device simulation which solves the drift diffusion model with the energy transport model and the tunnel current at the source heterojunction. However, this 2D simulator does not take the quasi-ballistic electron transport over the rapid potential step at the heterojunction into account. In this study, χ and L_H in SHOT structures were varied, but other physical properties of SHOT, such as the electron mobility, were assumed to be the same as those of Si. The SHOT in this work has SOI structure, as shown in Fig.1, and the SOI and the gate oxide thickness were taken to be 5nm and 1.5nm, respectively, to suppress the short channel effects in 15-nm channel length (L_{eff}). The channel dopant was $1\times10^{16}cm^{-3}$, and the buried oxide thickness was 100nm. Assuming that the supply voltage is 1V under nm-gate length region, we mainly focus on the design for SHOT in terms of G_m enhancement factors over that (G_0) of conventional SOI-MOSFETs with the same size; G_m/G_0.

III. ΔE_c Dependence

At first, Fig.3 shows the enhancement factors of the maximum G_m of SHOT compared to that of SOIs; G_m/G_0, as a function of the source heterojunction position from the source *pn* junction edge, where L_{eff} =15nm, V_d=1V, and ΔE_c=0.2eV. G_m is the maximum value, when the source heterojunction is located at around -6nm from the source *pn* junction egde, which is the optimized position of the source heterojunction. The reason why G_m decreases in SHOT with the heterojunction at around the *pn* junction edge is the larger barrier height formed in the conduction band profile as the dashed line in Fig.4.

Next, we discuss ΔE_c dependence of G_m/G_0 in 15-nm SHOT. Fig.5 shows the conduction band energy profile near the source region as a parameter of ΔE_c, at V_d of 1V. The peak energy level at the *pn* junction edge decreases with increasing ΔE_c. As a result, G_m enhancement due to the high velocity electron injection is expected to increase with the increase of ΔE_c. Fig.6 shows ΔE_c dependence of G_m/G_0 at L_{eff} of 15nm (solid lines) and 40nm (dashed lines). The 15nm devices (solid lines) show that G_m/G_0 increases with increasing ΔE_c and has the maximum value (~1.2) at ΔE_c of around 0.2eV. However, when ΔE_c is larger than 0.2eV, G_m/G_0 decreases with increasing ΔE_c even at V_d of 1V. This ΔE_c dependence of G_m/G_0 is explained as follows. Fig.7 shows the electron velocity distribution in the channel region and that the electron velocity is higher in the whole channel region at ΔE_c of 0.2eV than in conventional SOIs with ΔE_c of 0eV. However, the electron velocity in the channel is reduced at ΔE_c of 0.4eV, because the higher negative lateral electric field E_L (electric field from the drain to the source direction) at the heterojunction (Fig.8) is introduced by the higher ΔE_c and the resulting higher barrier height (Fig.5). Fig.6 also indicates that long L_{eff} devices (dashed lines) show small G_m/G_0 value even at V_d of 1V, because V_d of 1V is too low to realize high velocity electron injection at L_{eff} of 40nm. Consequently, it is necessary to optimize ΔE_c (0.2eV at L_{eff} of 15nm) to maximize the G_m enhancement.

IV. Graded Heterojunction Source Structure

We compare G_m enhancement of graded heterojunction SHOT to that of abrupt heterojunction structures at optimized ΔE_c. Fig.9 shows G_m/G_0 versus L_H at low (0.1V) and high V_d (1V), where ΔE_c=0.2eV. In the case of high V_d, G_m enhancement of abrupt heterojunction structures is larger than that of graded heterojunction ones. When L_H is long, the increase of E_L in the graded heterojunction is slow. As a result, non-stationary electron transport effect is mitigated in long L_H SHOT. Therefore, as shown in Fig.10, electron temperature (T_e) near the source becomes higher in long L_H SHOT, resulting in the electron velocity (v) decrease with increasing L_H. On the other hand, Fig.9 shows that G_m with L_H of around 5nm is enhanced even at V_d of 0.1V. This is due to the reduced barrier height at the graded heterojunction. The E_L distribution of the graded heterojunction, shown in Fig.11, indicates that the negative E_L peak decreases with increasing L_H. However, when L_H=10nm, the negative E_L regions expands, resulting in the electron velocity reduction. As a result, it is concluded that L_H has also the optimum value of around 5nm to realize larger G_m/G_0 in the wide range of V_d.

V. Optimum SHOT Structures

According to the above discussion on the optimized ΔE_c and L_H in SHOT, we can introduce the optimum design for high-speed SHOT. Fig.12 shows G_m/G_0 contour map in V_d-ΔE_c plane at L_H=2nm. The V_d dependence of G_m/G_0 is relatively small. When ΔE_c is between 0.15 and 0.25eV, larger G_m/G_0 can be achieved in the whole range of V_d, which is the optimum design for high-speed SHOT in 10-nm region.

In addition, when the channel of SHOT is composed of a strained-Si layer [1], the electron mobility enhancement can be also enjoyed. Fig.13 shows G_m/G_0 vs. ΔE_c in SHOT with the strained-Si channel, where ΔE_c and electron mobility enhancement depends on the strain value in the strained-Si layers [3], [4]. Compared to the G_m/G_0 value of SHOT without electron mobility enhancement shown in Fig.6, G_m/G_0 with strained-Si channels increases by about 20% at V_d of 1V. In particular, when V_d is 0.1V, G_m/G_0 has remarkable improvement at large ΔE_c which is due to the large electron mobility enhancement.

VI. Conclusion

We have studied device design of 15-nm high-speed SHOT with high velocity electron injection, using 2D devices simulation. ΔE_c and L_H of SHOT with the graded heterojunction structures have been optimized. As a result, the G_m enhancement due to high-velocity electron injection can be achieved in a whole range of V_d. The optimized SHOT is quite promising for high-speed CMOS devices under 10-nm regime.

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References: [1]T.Mizuno et al., *VLSI Symp.*, p.202 (2004). [2] K.W.Ang et al, *IEDM Tech. Dig.*, p.1069 (2004). [3] T.Mizuno et al, IEEE Trans., ED-50, 988 (2003). [4] M. Rashed et al., *IEDM Tech. Dig.*, p.765 (1995).

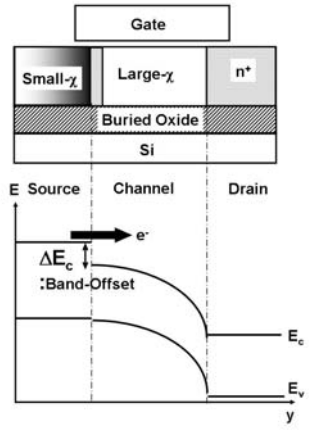

Fig.1 Schematic cross section of source-heterojunction MOS transistors (SHOT) and the band diagram. Inversion electron velocity is enhanced due to higher velocity electron injection by excess kinetic energy of the source band-offset ΔEc, using small electron affinity source and large electron affinity channel regions.

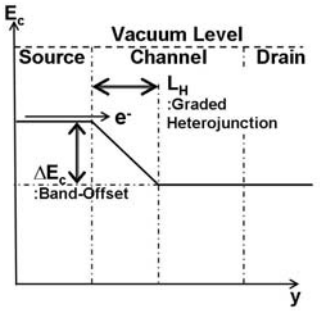

Fig.2 Schematic conduction band energy profile in SHOT. In this study, ΔEc and L_H are key parameters for realizing high-speed SHOT.

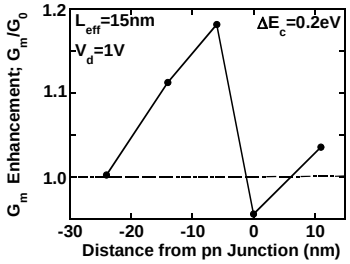

Fig.3 *Gm* enhancement factors compared to that of SOIs vs. the distance of source heterojunction edge from the source *pn* junction, where L_{eff}=15nm, ΔEc=0.2eV, and Vd=1V.

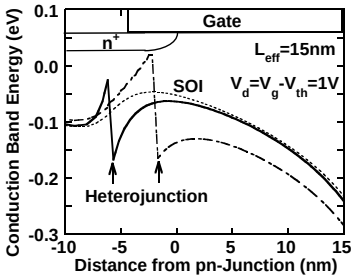

Fig.4 Conduction band energy profile of different heterojunction positions.

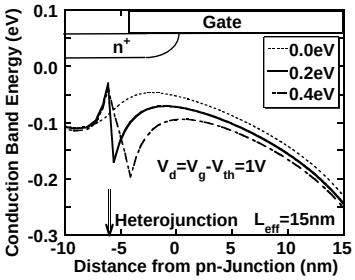

Fig.5 Conduction band energy distribution of SHOT with various ΔEc, where L_{eff}=15nm, and V_d=gate-drive=1V.

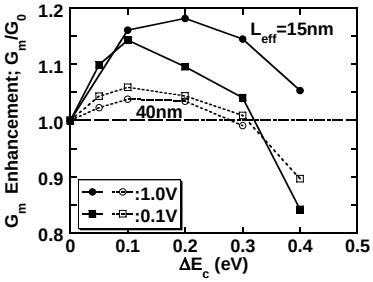

Fig.6 *Gm* enhancement vs. ΔEc. The solid and the dashed lines show the results at L_{eff} of 15nm and 40nm, respectively. Circles and squares indicate the data at V_d of 1V and 0.1V, respectively. *Gm* enhancement decrease at V_d of 0.1V is due to the high barrier height at the source heterojunction in the case of high ΔEc [1].

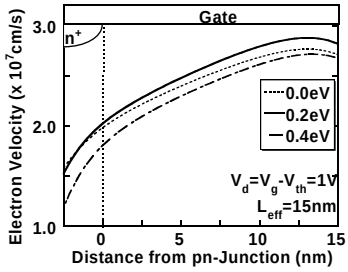

Fig.7 Electron velocity profile in SHOT, as the same conditions in Fig.5.

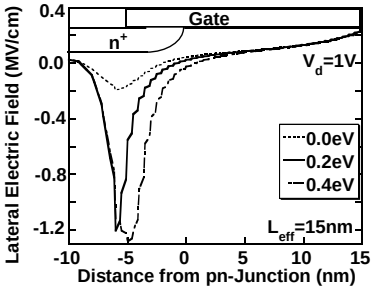

Fig.8 Lateral electric field in SHOT, as the same conditions in Fig.5.

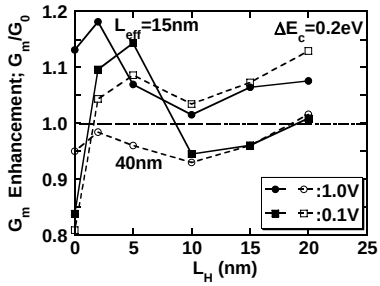

Fig.9 *Gm* enhancement as a function of L_H, where ΔEc=0.2eV. The solid and the dashed lines show the results of L_{eff} of 15nm and 40nm, respectively.

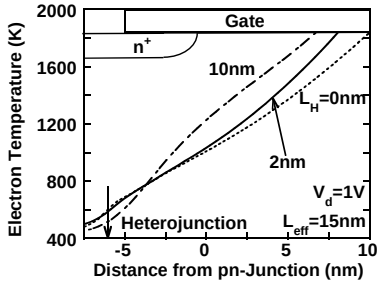

Fig.10 Electron temperature profile near the source region at V_d=1V, as a parameter of L_H.

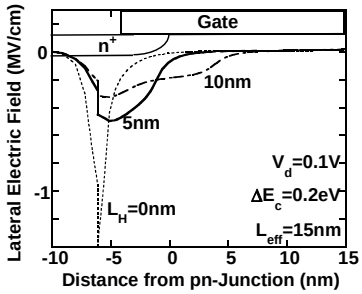

Fig.11 . Lateral electric field at Vd=0.1V, as a parameter of L_H.

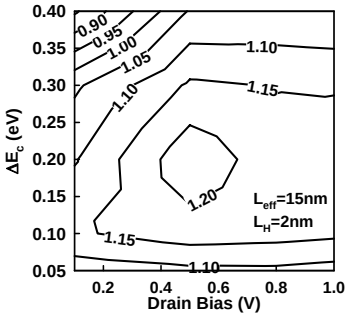

Fig.12 Contour map of *Gm* enhancement factors in 15-nm SHOT, compared to that of SOIs. The lateral and the vertical axes are the drain bias and ΔEc, respectively.

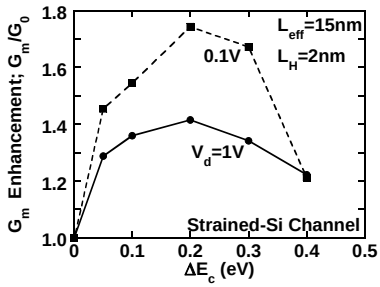

Fig.13 *Gm* enhancement factors vs. ΔEc in the case of the strained-Si channel at L_{eff} of 15nm.