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Mobility Increase in High-Ns Region in (110)-Oriented UTB pMOSFET Through Surface Roughness Improvement

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1. Introduction

Ultra-thin body (UTB) MOSFET with SOI layer thickness (t_{SOI}) below 10 nm is a strong candidate for future VLSIs thanks to its short-channel effect immunity. It has been reported that in (110)-oriented UTB pMOSFET with t_{SOI} of around 3 nm, mobility enhancement can be achieved by the quantum confinement[1]. However, it is known that (110) surface of Si is roughened more easily than (100)[2]. Therefore, it is predicted that surface roughness scattering may invoke significant mobility degradation in devices fabricated on (110).

In this study, we have successfully achieved higher hole mobility at the high-Ns region than our previously reported device[1], thanks to a better surface treatment during fabrication process. The origin of the mobility increase is investigated by experiment and calculation from the viewpoint of surface roughness limited mobility (μ_{SR}).

2. Fabrication and Extraction of Roughness Parameters

Fig. 1 shows the structure of the fabricated devices. The SOI-layer is thinned to around 3 nm by thermal oxidation and diluted HF etching. It is known that the roughness of (110) surface can easily increase even by mere dipping in ultra pure water[2], as confirmed in Fig. 2. In this work, two samples are compared. Device A is the device fabricated previously, and reported in [1]. Device B is a device fabricated with an improved process, i.e. with minimized dipping duration in ultra pure water during sample cleaning before gate oxidation.

The surface roughness of the SOI layer is measured by atomic force microscopy (AFM). Digital Instruments Nanoscope III Tapping Mode AFM with the smallest radius of curvature of the cantilever around 5 nm is used. Fig. 3 shows the AFM images corresponding to the silicon surface roughness of each device. The roughness parameters of each device are extracted from AFM data by fitting the one-dimensional height difference correlation function (Chd), as depicted in Fig. 4. The extracted values of the asperity height (Δ), correlation length (Λ), and Hurst exponent (H), are given in Table 1.

After performing all the electrical measurements, the SOI layer thickness of each device is determined by observing the TEM images. The cross sectional TEM image of both devices depicted in Fig. 5 shows very thin t_{SOI} of 3.6 nm and 3.0 nm for device A and B, respectively.

3. Mobility Comparison

The hole mobility of both devices is measured using the split-CV method. Fig. 6 shows the effective mobility measured at T=300 K and T=40 K. From the mobility data at T=300 K, it is clearly seen that at the high-Ns region, the hole mobility of device B exceeds device A, which is the device with the highest mobility among UTB devices with t_{SOI} = 3 nm reported to date[1]. The difference becomes more obvious and the clear Ns^{-1} dependence is observed at 40 K, where the phonon scattering is suppressed. These results suggest that the mobility is determined by μ_{SR} [4], rather than t_{SOI}-fluctuation scattering[5], and the mobility difference between devices A and B is likely to come from the difference in μ_{SR}. Therefore, we have considered the change in surface roughness to explain the mobility improvement, as discussed in the following.

4. Discussion

Table 1 shows that the asperity height of the surface roughness of both devices did not show any significant difference. However, some difference was observed in the roughness correlation length. It is known that for large correlation length satisfying $k_F\Lambda >> 1$ (k_F is the wavevector at Fermi energy), larger correlation length means higher roughness limited mobility [6]. It is confirmed that at high carrier concentration, $k_F\Lambda > 1$ is satisfied by both devices. Thus, the higher mobility of device B than device A is attributable to the larger correlation length, which is confirmed by a calculation as follows.

First, an autocorrelation function of the form :

$$S(r) = \Delta^2 \exp[-(r/\Lambda)^n] \qquad (1)$$

is assumed[7]. Using the single-subband relaxation-time approximation, the average value of momentum relaxation time $<\tau>$ at low temperature is approximated by the momentum relaxation time at the Fermi energy $\tau_m(k_F)$ [8]. Then, the ratio μ_{SR} of device A and B at low temperature is calculated by taking the ratio of $\tau_m(k_F)$ (because $\mu_{SR} \propto <\tau>$). In $\tau_m(k_F)$ calculation eq. (1) is used, with the roughness parameters as shown in Table 1. Calculation results are shown in Table 2. It is confirmed that higher mobility is obtained for device B due to a larger Λ. However, the calculation results were not adequate to explain the experimental results quantitatively. Two possible reasons which are not considered yet are the difference in t_{SOI}-fluctuation scattering and the cross correlation between the front interface and the back interface (SOI/BOX interface)[9], which become significant in devices with aggressively scaled SOI layer.

However, the result of this work implies that improvement of the front surface roughness seems to be still effective to increase high field mobility, even in ultra-thin SOI devices where the back interface plays important role in carrier scattering.

5. Conclusions

The hole mobility of (110)-oriented UTB pMOSFET at high-Ns region has successfully been increased through surface roughness improvement. It is shown that the mobility increase is partly attributable to the larger roughness correlation length. Device fabrication process with particular efforts to improve surface roughness will be increasingly important in the future.

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References

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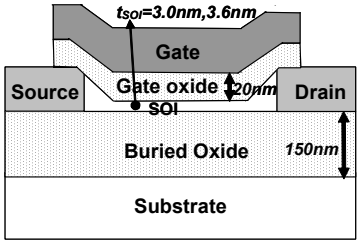


Fig. 1 : A schematic of fabricated (110)-oriented UTB pMOSFET.

Table 1. Extracted roughness parameters.

Parameters	Device A	Device B
Δ(nm)	0.26	0.26
Λ(nm)	11.0	14.9
H	0.77	0.66

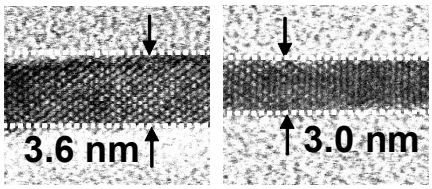
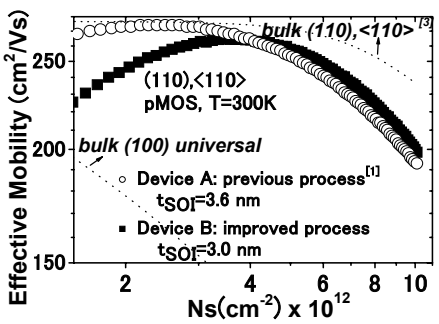


Fig. 5 :TEM image of fabricated devices : A (left) and B(right).



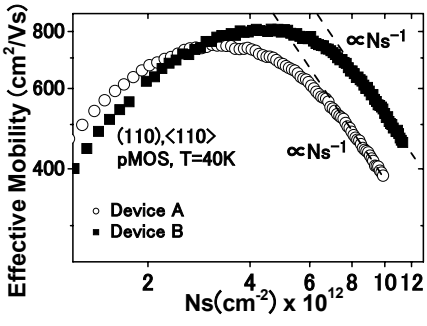
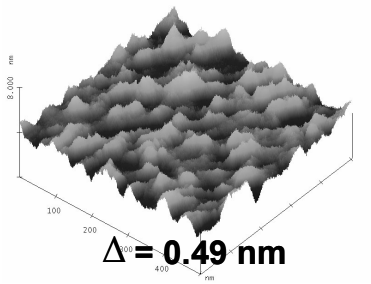


Fig. 6 : Measured effective mobility at T = 300 K (left) and T = 40 K (right).



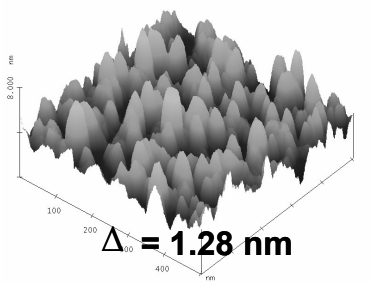
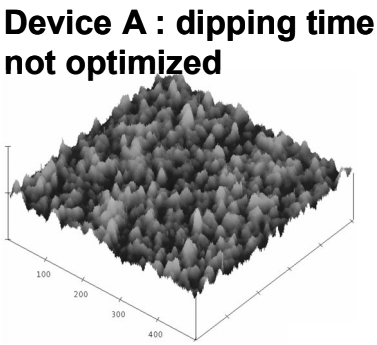


Fig. 2 : Surface roughness of (110) surface after RCA cleaning (left), and after 4 hours-dipping in ultra pure water following the RCA cleaning (right).



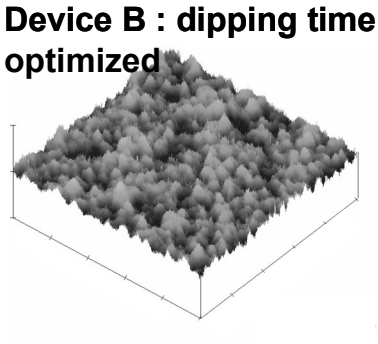
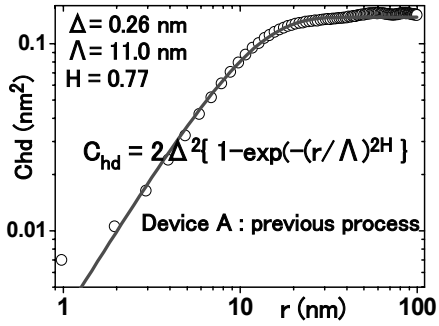


Fig. 3 : The AFM image of the surface corresponding to device A (left) and B (right), taken on 500 nm x 500 nm scan area. The surface roughness was observed after peeling the gate-poly Si and gate-oxide of the fabricated devices.



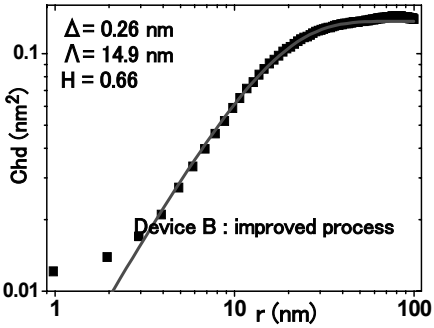


Fig. 4:The height-difference correlation function (*Chd*)of device A (left) and B (right), calculated from AFM data. *Chd* is defined as $< [h(r) - h(0)]^2 >$, where $h(r)$ is the surface height at the position r .

Table 2. Ratio of roughness limited mobility of device B and device A at low temperature. The rightmost row uses the measurement results at T=40 K.

Ns (cm^{-2})	Calculated	Measured
$8x10^{12}$	1.14	1.36
$9x10^{12}$	1.14	1.38
$1x10^{13}$	1.13	1.39