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Investigation of N-Channel Triple-Gate MOSFETs on (100) SOI Substrate

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Abstract

We have investigated the fabrication processes and device characteristics for the n-channel triple-gate MOSFETs on the (100) SOI substrate. We optimized the diagonal ion implantation condition for the narrow fin channel and the fabricated triple-gate device showed the electron mobility almost compatible with a planer MOSFET and a supreme subthreshold slope of 64 mV/decade and 15 mV DIBL.

1. Introduction

The power consumption issue in scaled MOSFETs becomes critical. Multiple gate MOSFETs offer a great potential in terms of their scalability in nano-scale CMOS technology thanks to their ability to suppress the leakage and maintain the high drive current[1]. Increasing number of the gate provides a better controllability of the channel potential. Thus, the triple-gate MOSFET is one of the promising candidates for future ULSI circuits[2][3]. However, there are many challenges for the triple gate MOSFET technology. Among them, the uniform distribution of the impurities across the vertical channel is one of the most important issues. In this paper, we investigate the advanced fabrication process using an optimized ion implantation, and demonstrate device characteristics for the n-channel triple-gate MOSFETs.

2. Fabrication of the Triple-gate Device

Process flow The process flow for the n-channel triple-gate MOSFET is summarized in Fig. 2. We used lightly dope p-type (100)-oriented silicon-on-insulator (SOI) wafers. The initial thickness of the SOI and buried oxide (BOX) layers were 100 nm and 200 nm respectively. A 50-nm-thick non-doped silicate glass (NSG) layer and the electron beam (EB) resist masks were formed to make hardmasks on the wafer. To fabricate the vertical Si-fins, the SOI layer was etched by a conventional reactive ion etching (RIE) using a Cl_2 inductively coupled plasma (ICP). To remove etch-related defects after the Si-fin etching, a sacrificial oxide was formed and removed by DHF prior to the 2-nm-thick gate oxidation at 850°C. The NSG mask on the Si-fin was removed coincidentally during the gate oxidation process. Then, the n^+ poly-Si gate was formed using EB lithography. After the gate formation, a shallow arsenic (As) implantation into the extension of the source/drain (S/D) was performed followed by a gate sidewall spacer formation, and a S/D implantation. The recrystallization annealing at 600°C and activation at 850°C for 30 minutes were carried out after the implantation.

S/D ion implantation On of the critical issues for the formation of the vertical channel MOSFETs is their dopant profile engineering. We used a ultrathin (1 nm) screening oxide and a 5 keV acceleration voltage for the S/D extension implantation to avoid the significant dopant loss, since significant numbers of the implanted As atoms remain in the thick (5 nm) screening oxide and the high energy As atoms are scattering out through the ultra thin channel [4],[5].

3. Device Results

Fig. 3 shows the SEM image of the triple-gate device after the gate etching. The triple-gate device with a gate length (L_g) of 100 nm was successfully fabricated. Fig. 4 shows the cross-sectional scanning transmission electron microscope (STEM) views of the single and multiple fins. The 2-nm-thick gate oxide was conformally formed around the Si-fins.

Fig. 5 shows the simulated crossectional contour plots for the as-implanted As concentration after the S/D extension implantation[6]. If As atoms would be implanted vertically, large fluctuation of the dopant profile would be anticipated regardless of the implantation energy as shown in Fig. 5(a), (b). Thus the diagonal implantation with a fifty-fifty dose in each side is required. However, the fluctuation in the As distribution does not dissolve with a 30°-tilted implantation. A 60°-tilted implantation enables us to distribute As atoms uniformly. Fig. 6 shows the simulated As profiles of the S/D region after the implantation and activation. The S/D layer containing above 10^{19} As atoms is amorphized during the implantation and we can not recrystallize the S/D without preserving the crystal seed layer. Fig. 6 (a) indicates that the seed layer is almost disappeared with the 50 keV implantation. Thus, we regulated the acceleration voltage to 30 keV to preserve a 30-nm-thick crystal seed layer. Fig. 6 (b) and (c) indicate that the S/D is successfully formed without a significant lateral diffusion below 850°C for 30 minutes. The lateral diffusion of As atoms to the channel was predicted to be 20 nm for the 850 °C activation in Fig. 6(c).

Fig. 7 shows the I_d-V_g characteristics of the triple-gate device with a L_g=100 nm. The predicted metallurgical L_g calculated from Fig. 6 was 60 nm. It should be noted that the subthreshold slope and the drain induced bias lowering (DIBL) of the small L_g device are successfully suppressed and show almost the ideal level. This indicates the effectiveness of the triple-gate for controlling the channel potential. Fig. 9 compares the effective electron mobilities between the planer and the triple-gate MOSFETs calculated from C_g-V_g and I_g-V_d curves in Fig. 8. The compatible mobility with the planer (110) MOSFET is achieved for the triple-gate device. Moreover, the peak mobility at the low gate voltage is higher for the tripe-gate device. This can be explained by the contribution from the higher mobility in the top (100) channel.

4. Summary

We have successful fabricated the n-channel triple-gate MOSFETs on the (100) SOI using a 60°-tilted ion implantation with a 1-nm-thick screening oxide and 5 keV acceleration. The fabricated device showed the electron mobility compatible with a planer (110) MOSFET and a supreme subthreshold slope of 64 mV/decade and 15 mV DIBL.

References

[1] T. Sekigawa et al., Solid State Elec. **27**, (1984) 827. [2] B. Doyle et al., VLSI Symp. 2003, pp. 133. [3] F. L. Yang et al., IEDM Tech. Digest 2002, pp.255. [4] M. Koh et al., SSDM 1998, Hiroshima, pp. 18. [5] M. Masahara et al., Appl. Phys. Lett. 85, (2004) 4139. [6] ATHENA, ATLAS, SILBVACO Int'l Inc.

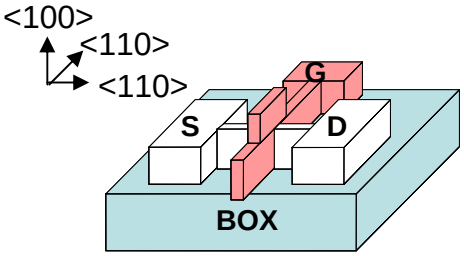

Fig.1. Schematic 3D view of the triple-gate MOSFET. Top and both sides of the thin Si-fin channels are surrounded by the gate electrode.

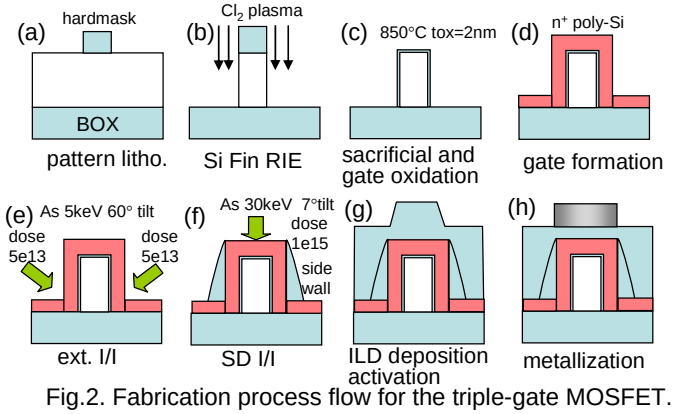

Fig.2. Fabrication process flow for the triple-gate MOSFET.

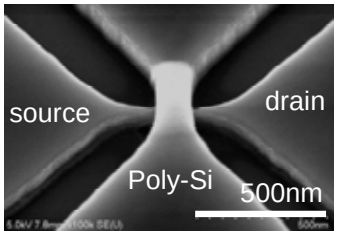

Fig.3. SEM image after the poly-Si gate etching.

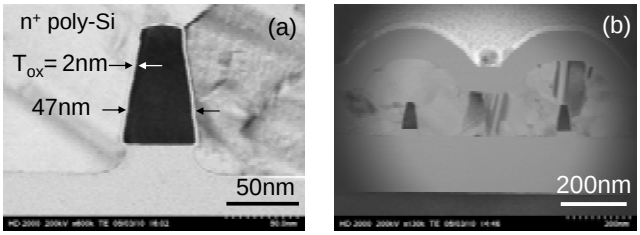

Fig.4. Crosssectional STEM images of the fabricated triple-gate MOSFETs.
(a) single fin (b) multi-fins

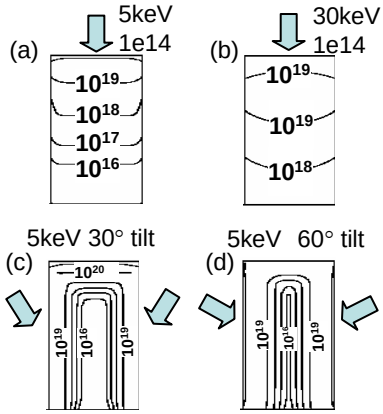

Fig.5. Simulated crosssectional dopant profiles at the extension region after the implantation corresponding to Fig. 2(e). (total dose:1e14)
(a) 0° tilt, (vertical) 5 keV, (b) 0° tilt, 30 keV, (c) 30° tilt, 5 keV, (d) 60° tilt, 5 keV

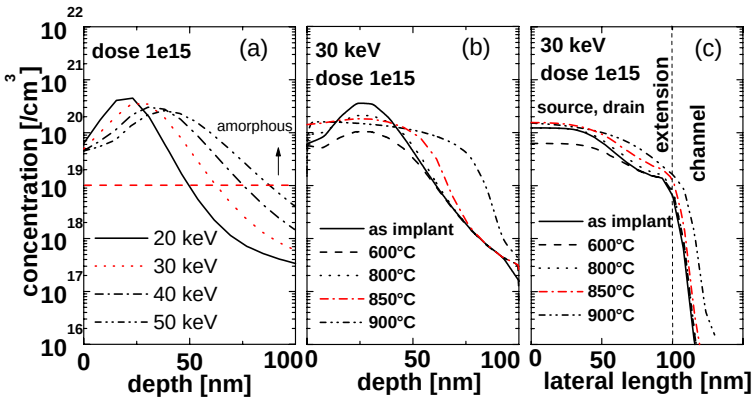

Fig.6. Simulated dopant depth profiles at the S/D region after the implantation and activation corresponding to Fig. 2(f),(g).
(a) vertical depth profiles with different acceleration energies
(b) vertical depth profiles with different annealing temperatures for 30 min.
(c) lateral distributions along the channel

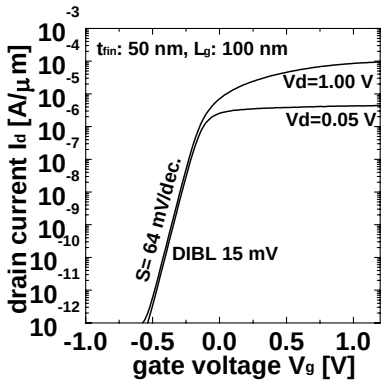

Fig.7. I_d-V_g characteristics of the fabricated triple-gate MOSFET. (t_{Fin}: 50 nm, L_g: 100 nm)

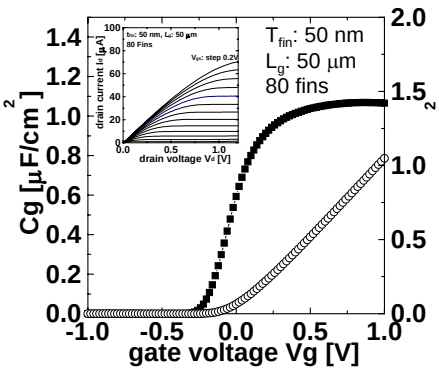

Fig.8. C_g-V_g and I_d-V_g characteristics of the fabricated multiple-channel MOSFET.

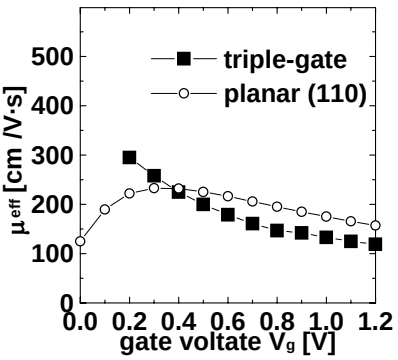

Fig.9. Comparison of the electron motilities for the triple-gate and planer MOSFETs as a function of the gate voltage.