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A Surrounding-Gate Transistor with Multi-Pillar Silicon Channels

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1. Introduction

Further scaling of CMOS devices faces formidable challenges due to the short-channel effects and lithographic limitations [1]. Among the numerous novel transistor schemes which have been suggested to overcome these difficulties, the surrounding-gate transistor has one of the best electrical characteristics and channel length scalability [2, 3] such as compared to the double-gate and other multi-gate transistors. However, these surrounding-gate devices still face lithographic pattern limitations. In this paper, a surrounding-gate transistor with multi-pillar channels is demonstrated. The transistor with a pillar diameter of 50nm has been successfully fabricated without the use of high-cost lithography.

2. Device structure

Fig. 1 shows the schematic diagram of the transistor demonstrated in this study. The transistor consists of multiple surrounding-gate silicon pillar channels. The top and bottom source/drain electrodes of the device are n+ silicon. The channel length is determined by the distance between two the source/drain junctions. Fig. 2 shows the equivalent circuit of the proposed and Fig. 3 indicates the cross-sectional view of the transistor along the a-a' direction of Fig. 1. The space between pillars are filled with the gate polysilicon, and electrically connected to each other. Since the the silicon pillar formation is defined by the anodization and electrodeposition, the lithography limitation is greatly relaxed for this device structure.

3. Device fabrication

For the fabrication of the device demonstrated in this study, Anodized Aluminum Oxidation (AAO) and electrodeposition technologies are used [4,5], enabling nano-scale patterning without using high-cost lithography. In order to form the hard masks for silicon pillar etching, nickel is electrically deposited in the pores formed by AAO. Anodized alumina is then removed by wet etching, leaving hard nickel masks on the silicon substrate. This technology enables us to fabricate 50nm of silicon pillars without deep sub-micron lithography technology.

Fig. 4 shows the device fabrication processing sequence. Nitride, titanium, and aluminum were deposited on silicon substrate with a resistivity of 10Ω-cm, followed by anodization in oxalic acid with a 0.3 molar concentration, as shown in Fig. 4(a). With an applied voltage of 30V, the pore diameter and pitch are 20nm and 80nm, respectively. The pore diameter was widened with a 5 Vol% of phosphoric acid dipping for 20 minutes. The widening process not only increases the pore size of the pillar, but also removes the barrier layer formed at the bottom of the pores after anodization. After electrically depositing nickel in the pores, anodized alumina was then removed by sodium hydroxide, leaving the nickel rods as a hard mask for subsequent silicon pillar etching as shown in Fig. 4(b) and Fig. 5(a). It was found that the nickel pillar diameter of 50nm is sufficient for masking the subsequent silicon etching. After the definition of the active region, the nickel rods in a field region were removed by nitric acid as shown in Fig. 4(c). The nickel rods at the edge of the active region are cylindrical in shape since the nitric acid etches all exposed pillars as shown in Fig. 5(b). The multiple layers of titanium, nitride, and silicon were etched by an Induction Coupled Plasma (ICP) RIE Etcher using the nickel as a hard mask. The nickel rods and titanium were then removed by wet etching as shown in Fig. 4(d). Next, gate oxidation and gate poly deposition were performed as shown in Fig. 6(a). After the definition of the gate poly-silicon mask, the gate poly was etched, leaving filled poly between silicon pillars as shown in Fig. 4(e). The gate poly oxidation was performed to prevent the gate poly from connecting to the subsequent top source/drain electrode as shown in Fig. 4(f). The nitride on top of the silicon pillar was removed by the phosphoric acid at 80˚C, followed by the top source/drain polysilicon deposition and patterning as shown in Fig. 6(b). The conventional Back-End-Of-Line process was performed as shown in Fig. 4(g).

4. Results and discussions

Fig. 7 shows the electrical characteristics of the device demonstrated in this study. Fig. 7(a) shows the I_{ds}-V_{gs} characteristic, and Fig. 7(b) shows the I_{ds}-V_{ds} characteristic for NMOS transistor with an active area of $3\mu m^2$. The drain current is 330μA per unit active area (μm^2) at V_{gs}=V_{ds}=1.5V for a channel length of 0.3μm, and gate oxide thickness of 6nm. The silicon pillar diameter and pitch (diameter plus space) are 60nm and 250nm, respectively. The drain current can be further improved when the pillar pitch is scaled. Fig. 8 shows the relationship between the drain current and the pillar pitch for several pillar diameters, indicating that the drain current is inversely proportional to the square of the pillar pitch when the pillar diameter is constant. The estimated drain current for the channel length of 0.3μm is $17mA/\mu m^2$ for a pillar diameter and a pitch of 20nm and 40nm, respectively. The drain current can be further improved by scaling the channel length and gate oxide thickness.

5. Conclusions

In this paper, a surrounding-gate transistor with multi-pillar silicon channels is demonstrated. The transistor has all the advantages of the surrounding-gate transistors such as improved short-channel effect and ideal subthreshold swing of 60mV/decade. Using anodization and electrodeposition technologies to form the hard masks for silicon pillar etching, this transistor does not have the patterning limitation of surround gate transistors proposed previously.

References

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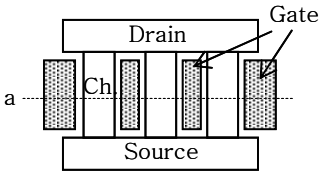

Fig. 1. Schematic diagram of the transistor with multi-pillar silicon channels.

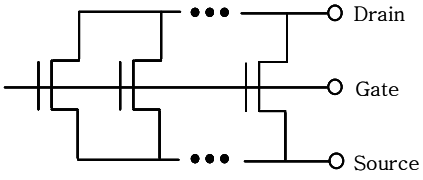

Fig. 2. Equivalent circuit of the transistor with multi-pillar silicon channels.

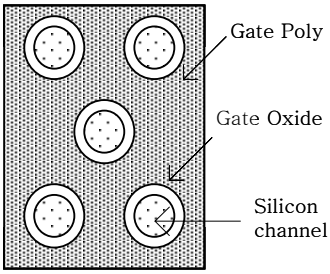

Fig. 3. Plane view of the transistor along a-a' cross-section of Fig. 1.

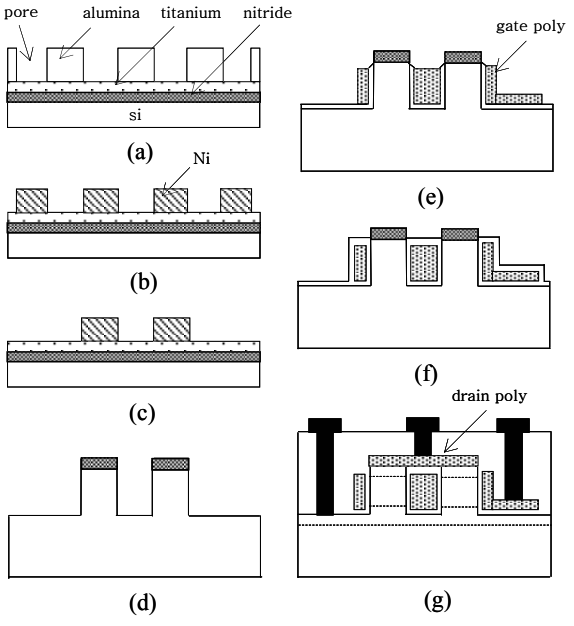

Fig. 4. Process sequence of the transistor with multi-pillar silicon channels.

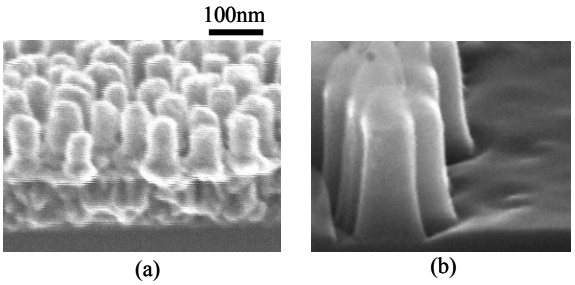

Fig. 5. SEM images for (a) nickel mask rods (b) silicon pillars along the edge of active region.

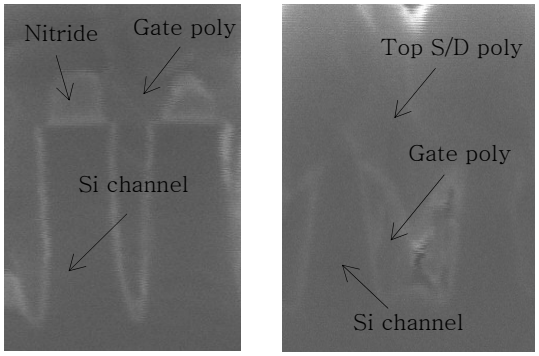

Fig. 6. SEM images for (a) silicon pillars after gate poly deposition (b) final transistor structure.

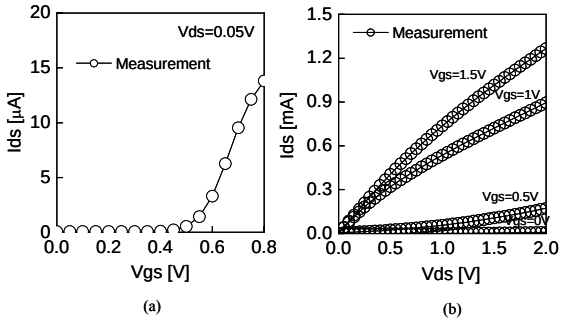

Fig. 7. Electrical characteristics of the device (a) Ids-Vgs curve (b) Ids-Vds curve.

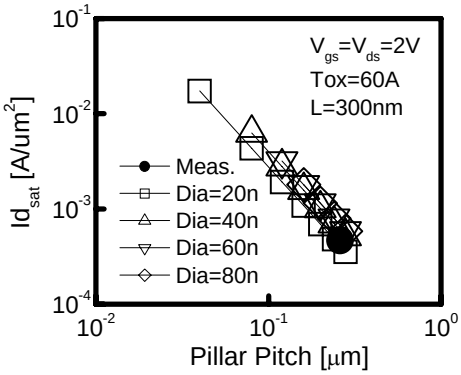

Fig. 8. Relationship between the drain current and the pillar pitch for different silicon pillar diameters.