

MOSFET Harmonic Distortion up to the Cutoff Frequency: Measurement and Theoretical Analysis

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1. Introduction

Scaling-down of MOSFETs has resulted to improved device cutoff frequency f_T which makes CMOS technology suitable for RF applications [1]. Accompanying these improvements are high-frequency-related phenomena occurring when the device is operated at RF switching. One phenomenon, important for RF designers, is harmonic distortion (HD) which exhibits the nonlinearity of MOSFETs. Up to now, HD investigations are still limited to relatively low frequencies [2] due to the fact that at high frequency, measurement becomes difficult and quasi-static-based (QS) MOSFET models are known to become inaccurate [3]. Our aim is to predict distortion characteristics at very fast switching. For this purpose, we measure and analyze the distortion characteristics of pocket-implanted, multi-fingered nMOSFETs with different channel lengths L_g from 1KHz to 10GHz input frequency. Analysis with HiSIM (Hiroshima-University STARC IGFET Model) [4] shows that at low drain bias, distortion characteristics are determined by the mobility of carriers. At high frequency, the charging of the channel becomes dominant and inclusion of non-quasi-static (NQS) effects becomes necessary to reproduce measurements. At high drain bias operation, distortion behaves fairly constant over a wide range of frequencies.

2. Harmonic Distortion Measurement System

Fig. 1 illustrates the principle of harmonic distortion. A sinusoidal input, with fundamental frequency f_0 , to a non-linear system like the MOSFET, produces not only f_0 but also its multiples, $2f_0$, $3f_0$, and so on, in the output signal. The amplitudes of these harmonics (HD1, HD2, HD3) are related to the MOSFET drain current I_{ds} by

$$\text{HD1} \propto \frac{\partial I_{ds}}{\partial V_{gs}} \quad \text{HD2} \propto \frac{\partial^2 I_{ds}}{\partial V_{gs}^2} \quad \text{HD3} \propto \frac{\partial^3 I_{ds}}{\partial V_{gs}^3}. \quad (1)$$

Shown in Fig. 2 is the system we used to perform distortion measurements. The input sinusoidal gate voltage V_{in} is equal to $V_{gs} + V_p \sin 2\pi f_0 t$, where V_{gs} is the DC offset, V_p is the amplitude of the sinusoidal input fixed at 50mV. In the circuit, high frequency noise coming from the voltage source is filtered first before entering the MOSFET. The output AC current and its associated harmonics are detected by a spectrum analyzer.

3. Measured Distortion Results and

Analysis with HiSIM

A. Low frequency input. Fig. 3 shows measured HD characteristics of a $0.5\mu\text{m}$ -nMOS for a 1KHz input frequency. Using HiSIM-QS, only measured DC I - V characteristics are fitted. Analysis with HiSIM shows that at low drain bias and low frequency, the HD characteristics are directly related to the mobility of carriers as shown in Figs. 4a and b. The minima of HD curves correspond to the minima of the mobility curve as depicted by the vertical lines.

Mobility is modeled using the universal mobility model. Moreover, the locations of the HD minima are very much sensitive to a change in mobility parameters as demonstrated in Fig. 5 where the surface roughness parameter is changed by 5%. Therefore, mobility is the dominant factor which determines the distortion characteristics under this condition.

B. High frequency input. At cutoff frequency operation, we measured the HD characteristics of a $5\mu\text{m}$ -nMOS ($f_T = 200\text{MHz}$) at 1MHz, 100MHz and 1GHz switching. As f_0 is increased, a notable observation is the flattening of the first harmonic HD1 as shown in Fig. 6a, which is attributed to the increasing effect of the charging current relative to the conductive current. Charging current also includes the charging of the MOSFET overlap region. Another observation is that as f_0 increases, the point where HD1 starts shifts to higher gate voltages as depicted by the arrows in Fig. 6a. This explains the fact that as the switching time shortens down to the carrier time delay for charging and discharging of the channel, the MOSFET-output current follows the applied gate voltage change only at sufficiently higher V_{gs} .

In order to reproduce the measured results, it is necessary to include the NQS effect in HiSIM. The NQS effect originates from the time delay of the carriers to form the channel, which is explicitly modeled in HiSIM-NQS [5, 6]. Reproduction with HiSIM-NQS is achieved as shown in Fig. 6b. Oscillations occurring at low voltage are due to the accuracy limit of SPICE3 simulator we used. The resulting NQS effects on the drain current are reduction of the current amplitude and introduction of phase delay as shown in Fig. 7. Therefore, under low V_{ds} and high frequency, the charging current accompanied by the carrier delay influences HD characteristics.

At saturation condition, the HD characteristics are fairly constant over a wide range of frequencies below f_T as shown in Fig. 8a for a shorter gate length. Under this condition, the transport of carriers is strongly governed by the field E_y along the channel caused by the drain voltage. HiSIM-calculated result reproduces the measured distortion characteristics as shown in Fig. 8b.

4. Summary

Harmonic distortion characteristics up to the cutoff frequency are measured and analyzed with the MOSFET model HiSIM. Carrier mobility determines the distortion characteristics at low input drain bias and low frequency. At high frequency, the carrier time delay influences the distortion characteristics and application of non-quasi-static effects is necessary to reproduce the measurements. Our results are useful for RF designers to accurately predict distortion characteristics over a wide range of input voltages and frequencies without direct measurement.

References

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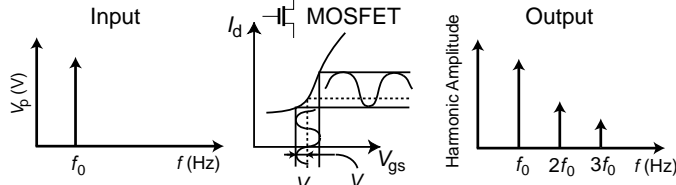


Fig. 1. Schematic illustration of harmonic distortion. A sinusoidal input in a nonlinear system such as the MOSFET produces harmonics in the output.

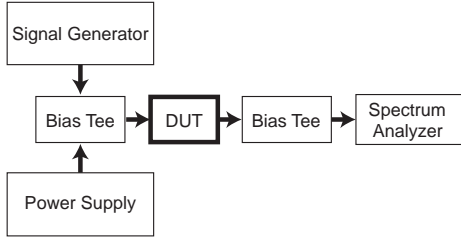


Fig. 2. Block diagram of the system used in measuring harmonic distortion. The input signal to the MOSFET (DUT) contains AC and DC components coming from the signal generator and power supply, respectively, which are combined by the first bias tee. The MOSFET output signal is then filtered by the second bias tee and the AC component is detected by the spectrum analyzer.

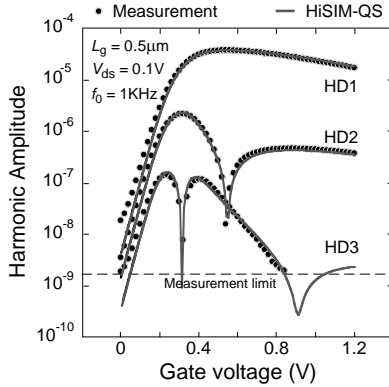


Fig. 3. Measured low frequency harmonic distortion characteristics in comparison with HiSIM-QS. Good agreement is achieved without any fitting parameter.

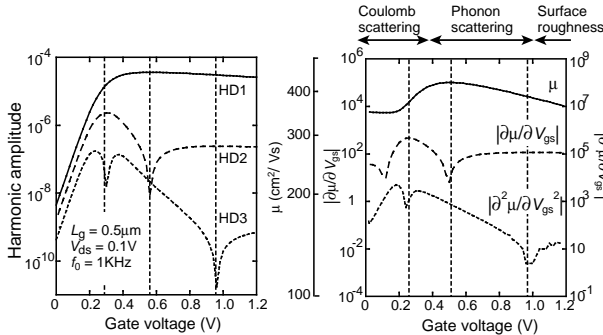


Fig. 4. (a) Low frequency harmonic distortion characteristics depicting the location of minima. (b) Mobility determines the location of distortion minima.

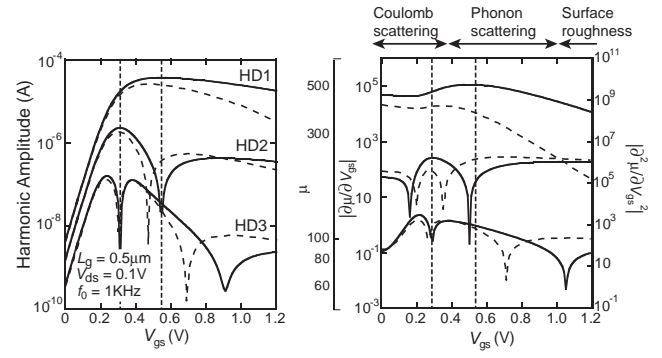


Fig. 5. HD characteristics are very sensitive to a slight change in the surface roughness model parameter.

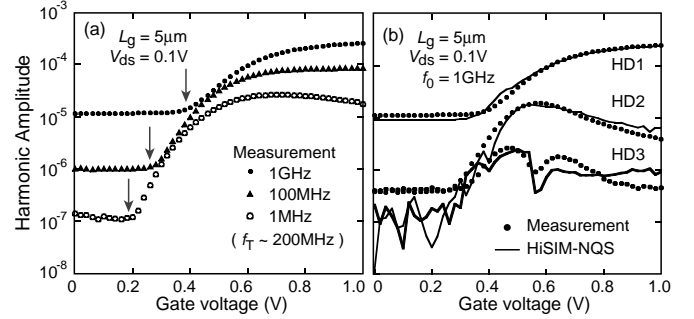


Fig. 6. (a) As the input harmonic frequency increases, HD1 flattens due to increasing effect of charging current. Moreover, the point where HD1 starts to shift to higher voltages which exhibits the carrier time delay for charging and discharging of the channel. (b) Measured harmonic distortion at cutoff region in comparison with HiSIM.

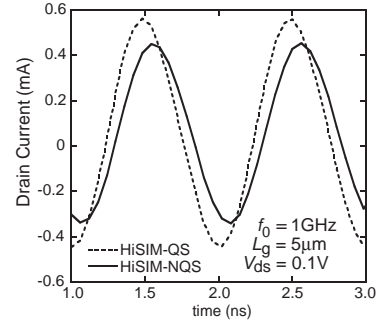


Fig. 7. HiSIM-QS and -NQS transient drain current results. NQS effects are reduction of amplitude and introduction of phase delay.

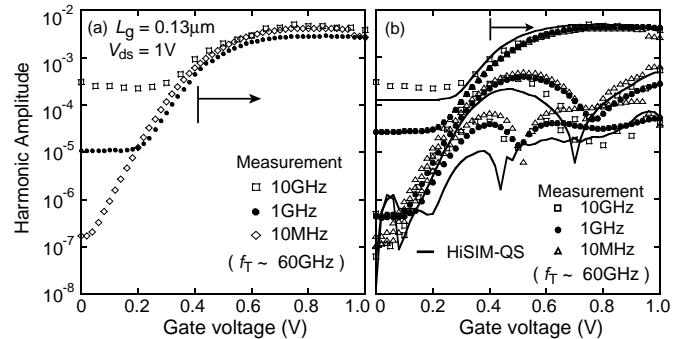


Fig. 8. (a) HD characteristics are fairly constant with respect to frequency at saturation condition (high V_{ds} and V_{gs}) as depicted by the arrow. (b) HiSIM calculated distortion in comparison with measurements.