B-6-2

Modeling of Body Factor and Subthreshold Swing in Short Channel Bulk MOSFETs

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1. Introduction

When designing a variable-threshold-voltage CMOS (VTCMOS) [1], the body factor γ defined by dV_{th}/dV_{bs} is one of the most important parameters and a sufficiently large value of γ is required [2]. The relation between subthreshold swing (S) and γ in a long channel device is given by [2]:

$$S = 60(1+\gamma) \quad (1)$$

In a short channel device, however, this simple relation no longer holds and a new model is strongly required. An analytical expression of relation between γ and S in short channel bulk MOSFETs has been reported recently [3]. However, it only discussed at low drain voltage (V_{dd} = 0.1 V), the models were complex, and the physical characteristics hidden in γ and S are still unclear.

In this paper, we present simple empirical models of γ and S at low and even high drain voltage. The models are verified by comparing with results of 2D device simulation [4]. The relation between γ and S in a short channel device at the presence of high drain voltage is derived for the first time.

2. Proposed Models

Fig. 1 shows the device structure assumed in this work [5]. t_d corresponds to the depletion width and γ is changed by varying t_d. We use a capacitance network model shown in Fig. 2 [6]. C_G, C_B, C_D and C_S are gate, substrate, drain, and source to channel capacitances for unit width, respectively. When the channel length becomes shorter, C_G/L and C_B/L (unit area capacitance) start to decrease by the short channel effect (SCE):

$$C_G / L = (C_{G0} - \alpha / L^2) \quad (2) \qquad C_B / L = (C_{B0} - \beta / L^2) \quad (3)$$

where C_{G0} and C_{B0} are gate and substrate capacitance per unit area in a long channel device, respectively, which are shown as

$$C_{G0} = \varepsilon_{OX} / t_{ox\_ele} \quad (4) \qquad C_{B0} = \varepsilon_{Si} / t_d \ , \quad (5)$$

α and β are parameters caused by SCE, L is the gate length, and t_{ox_ele} is electrical equivalent thickness of the gate oxide [7]. We assume that in a short channel the effect of α can be ignored due to very close distance between gate and channel, while β should be taken into account.

We also consider that DIBL causes the maximum potential barrier to move from the center of the channel towards the source as shown in Fig. 3, and consequently C_D decreases and C_S increases as,

$$C_S = k\varepsilon_{Si}\, t_d x_j /(L/2 - \Delta x)^2 \quad (6)$$

$$C_D = k\varepsilon_{Si}\, t_d x_j /(L/2 + \Delta x)^2 \quad (7)$$

where Δx is the distance shifted toward the source by DIBL, k is a fitting parameter, and x_j is metallurgical depth.

3. Derivation of Body Factor and Subthreshold Swing

γ is determined approximately by C_B/C_G, which means the ratio of the effect of substrate bias on the channel to that of the gate voltage. On the other hand, S is determined by the ratio of the total capacitance of the channel to C_G. This assumption is valid in both long and short channel:

$$\gamma = \frac{C_B}{C_G} \approx \frac{C_{B0}}{C_{G0}} - \frac{\beta}{C_{G0}L^2} = \gamma_0 - \Delta\gamma \quad (8)$$

$$S = \frac{S}{60} = \frac{(C_B + C_G + C_S + C_D)}{C_G} \cong \left(1 + \frac{C_{B0}}{C_{G0}}\right) + \frac{(C_S + C_D)/L - \beta/L^2}{C_{G0}} = S_0 + \Delta S \quad (9)$$

where $\Delta\gamma$ and ΔS are the differences of γ and S between long and short channel devices. By substituting eq. (4), (6), (7) into (8) and (9), we obtain $\Delta\gamma$ and ΔS as follows.

$$\Delta\gamma = A / L^2 \quad (10)$$

$$\Delta S = \frac{Bt_d}{L}\left(\frac{1}{(L/2 - \Delta x)^2} + \frac{1}{(L/2 + \Delta x)^2}\right) - \frac{A}{L^2} \quad (11)$$

where $A = \beta t_{ox\_ele} / \varepsilon_{ox}$ and $B = kt_{ox\_ele}\, x_j \varepsilon_{Si} / \varepsilon_{ox}$. The model is fitted to the device simulation results. The device parameters are based on hp90 LSTP devices of 2003 ITRS [8]. A, B, and Δx are 210 nm^2, 144 nm^2, and 7.5 nm, respectively.

4. Results and Discussion

Figs. 4 and 5 show gate length dependence of S and γ, respectively. The model and the simulation are compared, and a good agreement is obtained. S increases and γ decreases by SCE. When applying high drain voltage, S is severely degraded due to DIBL as shown in Fig. 4(b). However, it is interesting to note that the degradation of γ does not depend on DIBL, as shown in Figs. 5 (a) and (b). This is because according to eq. (8) γ is not related to C_D and C_S. Simulated gate length dependence of DIBL is shown in Fig. 6. The value of DIBL reaches 200 mV/V at L = 40 nm. Therefore, it is shown that our model is valid in the range where DIBL < 200 mV/V.

Finally, the relation between S and γ in a short channel device at high drain voltage is derived as a simple form:

$$S = 60\left[1 + \gamma + \frac{Bt_d}{L}\left(\frac{1}{(L/2 - \Delta x)^2} + \frac{1}{(L/2 + \Delta x)^2}\right)\right]. \quad (12)$$

The third term in parenthesis corresponds to the correction due to SCE and DIBL. Fig. 7 shows the comparison of the model and simulation in the relation between S and γ in long and short channel devices. In a long channel device (L = 500 nm), eq. (1) is valid, as shown in the figure, and S is the smallest when γ = 0. As L becomes shorter, S gradually becomes larger than the line of eq. (1), and S is severely degraded when L = 40 nm especially in the small γ regime due to SCE. Please note that S exhibits the minimum value at a certain value of γ (around 0.25 when L = 50 nm). This result indicates that the optimum design of γ is very important for LSTP devices, and the present model will help the device design.

5. Conclusions

We have proposed empirical models of body factor and subthreshold swing in short channel devices at not only low but high drain voltage. This model is very effective for the design of variable threshold-voltage CMOS circuits.

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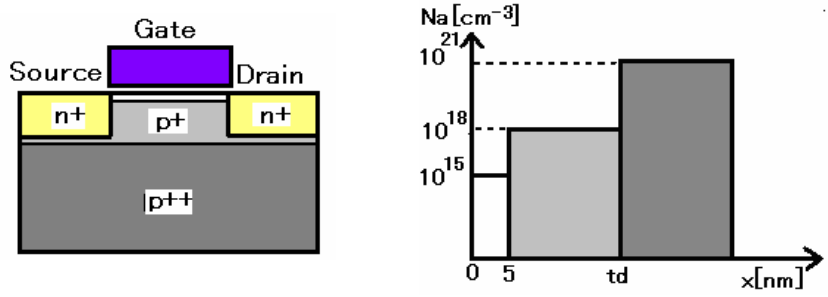


(a) (b)

Fig. 1. (a) A schematic of the device structure assumed in this study. An ideal step-like profile is assumed, where the depletion width (W_{dm}) is determined by the depth of the upper layer (t_d) with low impurity concentration. In this device structure, Vth and γ are independently varied. (b) Profile of impurity concentration in the assumed device.

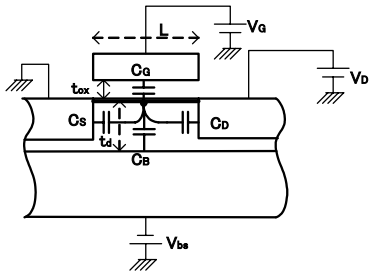


Fig. 2. A schematic of the capacitance network model. We consider C_G, C_B, C_S, and C_D as gate, substrate, source, and drain to channel capacitances for unit width, respectively.

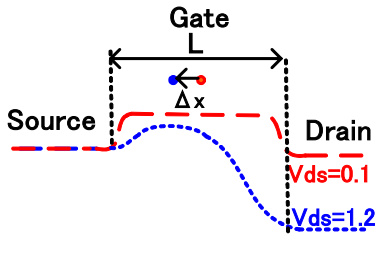
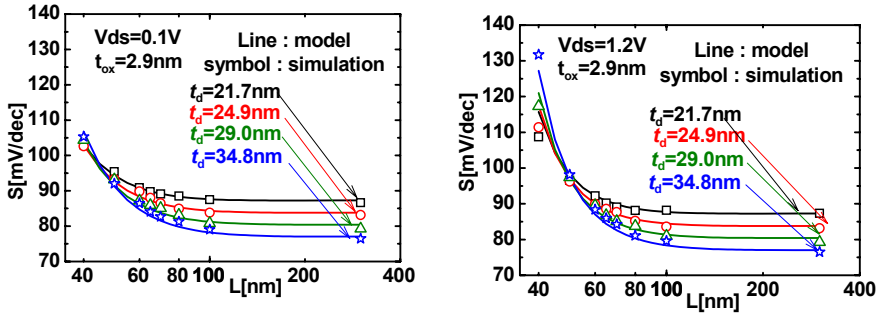
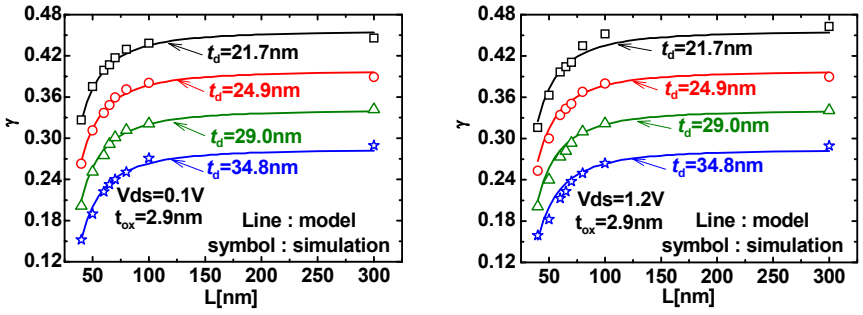


Fig. 3. A schematic of channel potential profile. At a low *V*ds the maximum of the potential barrier is at the center, while at a high *V*ds it moves toward the source due to DIBL.



(a) (b)

Fig. 4. Comparison of the model and 2D simulation in gate length (L) dependence of subthreshold factor (S). (a) *V*ds = 0.1 V where DIBL can be neglected. (b) *V*ds = 1.2 V where DIBL takes place.



(a) (b)

Fig. 5. Comparison of the model and 2D simulation in gate length (L) dependence of body factor (γ). (a) *V*ds = 0.1 V where DIBL can be neglected. (b) *V*ds = 1.2 V where DIBL takes place.

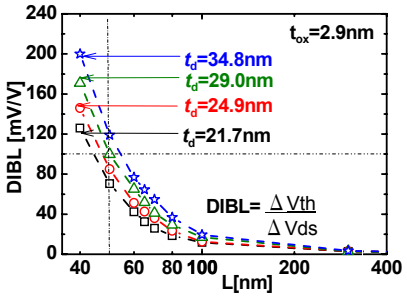


Fig. 6. Simulated gate length dependence of DIBL. DIBL exceed 100 mV/V when L < 50 nm.

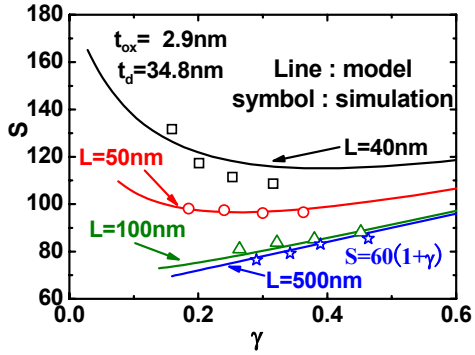


Fig. 7. The relation between S and γ in devices with different gate lengths. The model and 2D simulation are compared. When L is long enough (L=500 nm), the relation between S and γ is S =60(1+γ). However, as L is reduced, S becomes larger than the line of S =60(1+γ) due to SCE. It should be noted that S has the minimum value at a certain value of γ in short channel devices, indicating that the optimum design of γ is very important.