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Capacitance Due to the Charge Layer Thickness in Nanoscale Capacitors

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1. Introduction

It is well known that down-sizing of MOSFETs has disclosed critical importance of the inversion layer capacitance[1] for device operation. In recent nanoscale transistors, the performance degradation due to capacitance of the polysilicon gate depletion[2] has been pointed out, and it constitutes a serious problem leading to urgent investigation for the metal gate MOSFETs.

In this paper, "the third capacitance of nanoscale MOSFETs" due to thickness of the charge layer in the gate electrode is discussed. The capacitance is caused by the fact that the electrode charge distributes in a non-zero thickness layer[3], contrary to the case of a perfect conductor, as is illustrated in Fig. 1. The electric potential inevitably varies within the thickness and causes a capacitance component. It is a quantum effect, and is found both in the poly-silicon and the metal electrode, although the poly-silicon case is more conspicuous. As is expected, the effect is more serious for the thinner and the higher-k gate-insulator capacitors, as is exemplified in recent nanoscale transistors. The effect has a long history in various fields[3]. Recently, Black[4] has discussed the effect in metal electrodes in terms of the carrier screening length. We evaluate the effect for the case of capacitor plates with free electrons in a jellium electrode model by means of the Hartree approximation, and found that the effect is very serious for nanoscale capacitors.

2. Analysis

We analyze for convenience a symmetric structure with two capacitors tied together back to back as shown in Fig. 2, and focus on carriers on the central electrode forming a capacitor plate. Assuming free particle motion of carriers along interface of the plate, we solve the coupled Schrodinger equation and Poisson equation in z-direction perpendicular to the interface. The central electrode constitutes a potential well in z-direction, and the confined electrons are accommodated in energy levels. We have assumed the thickness of electrode is 10 nm, and the donor concentration is 1.2×10^{20} /cm^3. The potential barrier forming the well is assumed to be 3.1 eV, although the case of infinite barrier height without any carrier penetration into insulator is also analyzed. The valley structure of n-Si conduction band is considered and various crystal planes of the electrode are discussed. Some wave functions of lowest energy levels for (100) interface are plotted in Fig. 4. The charge distribution in the electrode is obtained as a sum of the electronic charge and the donor ionic charge forming the jellium. The self-consistent potential energy distribution obtained by the Hartree approximation is as shown in Fig. 5. In terms of the induced electrode charge Q estimated from the wave function, as well as the potential variation V across the charge layer, we can estimate the capacitance of the layer as $C=dQ/dV$. The induced charge distribution in the electrode for a potential increment of 2 mV from the zero bias condition (zero charge electrode) is evaluated as shown in Fig. 6. We see the increment charge distribution extends to roughly 3-4 nm into the electrode. The capacitance due to the charge distribution is plotted in Fig. 7, and it takes a value of 3.35 Å expressed in the effective oxide thickness (EOT). The carrier confinement and the energy level are dependent on width of the potential well (thickness of the electrode) and the thickness dependence of the capacitance is investigated. The thickness of electrode is varied from 10 nm to 20 nm in several points, but the induced charge distribution as well as the resultant capacitance component little changed and the present result is shown to be general and independent on the thickness. Real poly-silicon gate consists of crystal grains and lots of crystal planes face the interface. The capacitance value averaged over lots of crystal planes gives a value of 3.55 Å. The inversion layer capacitance for (100) interface is estimated to be 5-6 Å (EOT)[1]. The present capacitance is slightly larger as suggested by the reduced EOT value, but a similar serious effect on device operation is expected. The gate depletion capacitance is expected negligible for the gate doping of $N_d\sim10^{20}$ /cm^3[2]. The present capacitance still persists for the doping, and a larger EOT will result if the gate bias is increased so as to get a strong channel inversion, because the electronic concentration near the electrode interface is repelled and reduced, and the thickness of the charge layer is enhanced. The present capacitance for a metal electrode is interested. For the Cu gate with an increased electronic concentration, a simple estimation with the infinite barrier height of the well gives a EOT value of 1.36 Å.

3.Conclusion

The capacitance due to the charge distribution in the nanoscale capacitor plate was investigated. The capacitance

of a poly silicon gate with the doping concentration 1.2×10^{20} /cm^3 amounts to 3.55 Å in EOT value. The magnitude is in the same order as in the inversion layer capacitance, and the effect is serious also in the region where the gate depletion effect is negligible. For a metal Cu gate a simple estimation gives a EOT value of 1.36 Å.

References

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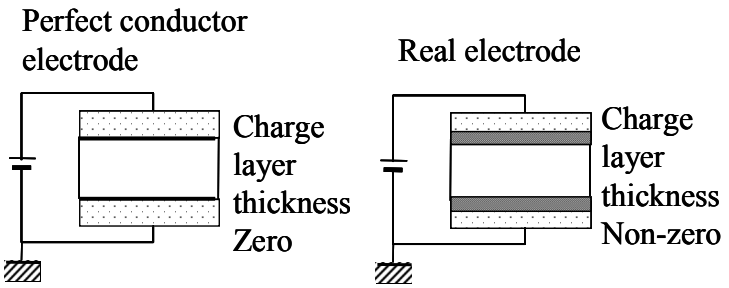

Fig. 1. In real capacitor electrodes, the induced charge has a finite thickness and causes capacitance.

$$\left\{\frac{\hbar^2}{2m}\frac{d^2}{dz^2}+q\phi(z)\right\}\zeta_i(z)+E_{zi}\zeta_i(z)=0$$

$$\frac{d^2\phi(z)}{dz^2}=\frac{\left\{q\sum_i N_i\left|\zeta_i(z)\right|^2-\rho^+\right\}}{\kappa\varepsilon_0}$$

$$C=\frac{dQ}{dV}$$

Fig. 3. Analytical formalism.

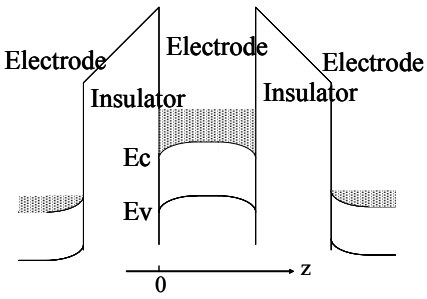

Fig. 2. The band structure of the analyzed device.

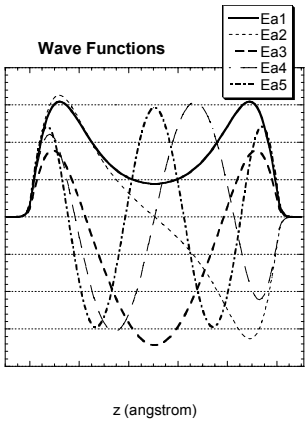

Fig. 4. Some lower level wave functions for the (100) interface.

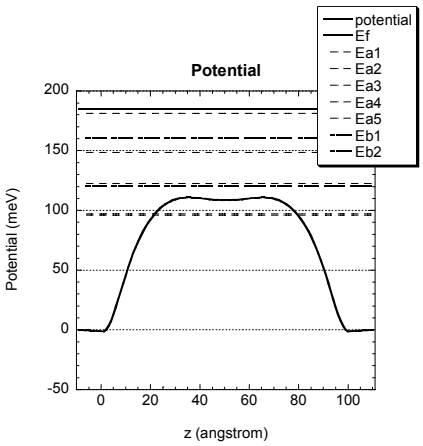

Fig. 5. Potential energy profile and some energy levels for (100) interface.

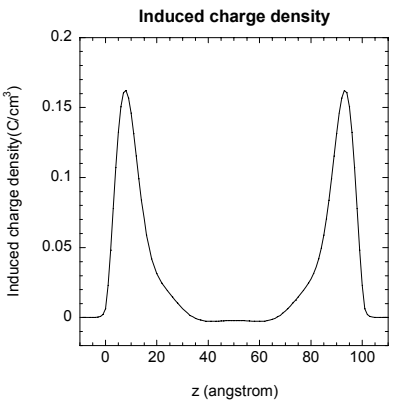

Fig. 6. The induced charge layer has a considerable thickness. ((100) interface)

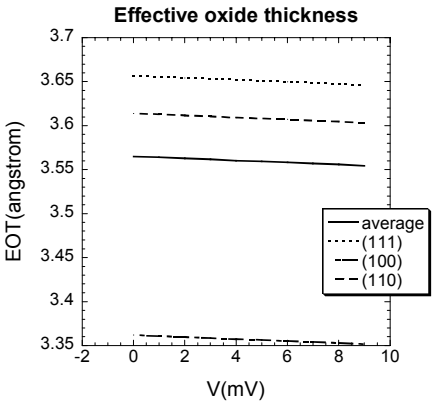

Fig. 7. Capacitance of electrode charge layer in effective oxide thickness.

Table I. Comparison of parasitic capacitances of nanosle capacitors.

	EOT (Å)
Charge layer Cap.	
Poly-silicon gate	3.55
Cu gate	1.36
(Infinite barrier well)	
Inversion capacitance	5-6