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P-channel Vertical Tunnel Field-Effect Transistors Down to Sub-50 nm Channel Length

Krishna K. Bhuwalka[1], Mathias Born, Markus Schindler, Matthias Schmidt, Torsten Sulima, and Ignaz Eisele

Institute of Physics, Universität der Bundeswehr, Munich 85577 Neubiberg Germany
[1]Ph: +49 89 60044043, Fax: +49 89 60043877, Krishna.K.Bhuwalka@UniBw-Muenchen.de

I. Introduction

Lateral as well as vertical gated p-i-n diodes, operating as surface tunnel transistors have been proposed as an alternative to future scaled CMOS technologies [1]–[5]. The p-i-n diode structure results in very low leakage current, I_{off}. Further, the $I-V$ characteristics is weakly dependent on temperature, T, and is nearly independent of the i-zone, which determines the channel length, L of the device. Symmetric source and drain doping with mid-bandgap gate material result in symmetric preformance. To overcome the low I_{on} current of Si tunnel FETs, we proposed significant performance improvement with SiGe [6]. It was further observed that the tunnel FETs can be optimized to have a sub-60 mV/dec room temperature swing. Thus, allowing scaling of these devices with large I_{on}/I_{off} ratios [7]. In this abstract, we present, for the first time, experimental verification of p-channel tunnel FETs down to i-zone of 70 nm and 25 nm.

II. Results and Discussion

The devices are grown by epitaxy by LPCVD under identical conditions, with t_{ox} =4.5 nm, and p-polysilicon as gate electrode. The schematic and SIMS doping profile for 25 nm i-zone device are shown in figures 1 and 2, respectively. Fig. 3 shows the transfer characteristics at T=293 K for the 70 nm device. While I_{DS} increases exponentially, I_{off}=250 fA/μm. This is more than 3 orders of magnitude less than the technology requirement for the 70 nm channel length. Normalized I_{on} at $|V_{GD}|/t_{ox}$=1 V/nm is 1μA/μm. Thus, yielding an excellent I_{on}/I_{off} ratio of more than 10^6. It should be noted, that even though the I_{on} is low as compared to the industry requirements, it is the highest achieved for vertical tunnel FETs. Figures 4 and 5 show the transfer characteristics at low and high temperatures, respectively. While I_{on} and V_T are weakly dependent on temperatures down to 33K, swing, S, is independent of T. Thus, the carrier mobility and hence the channel does not play any role in the $I-V$ characteristics. Weak positive temperature coefficient in the $I-V$ curves is due to the dependence of bandgap on T. A kT/q independent S is advantageous, as unlike the conventional MOSFETs, it allows the possibility of optimizing the devices with a sub-60 mV/dec room-temperature swing [6]. Fig. 6 shows the p-channel transfer characteristics for L =25 nm. Since the device is processed under identical conditions as the L =70 nm tunnel FET, it shows an identical and L independent I_{on} and V_T. As the device is not optimized for the 25 nm i-zone, the doping smear-out in the channel result in an early p-i-n diode Zener breakdown, leading to exponentially increasing I_{off} with V_{DS}. Further optimization can be done by having a sharper doping profile and thinner t_{ox}.

References

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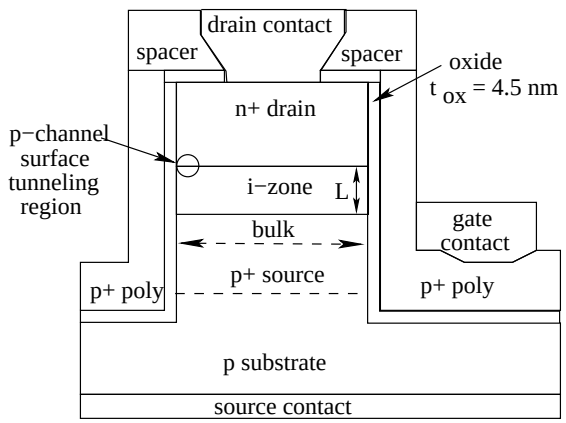

Fig. 1. Schematic representation of the tunnel FET. P-channel surface tunneling region is indicated.

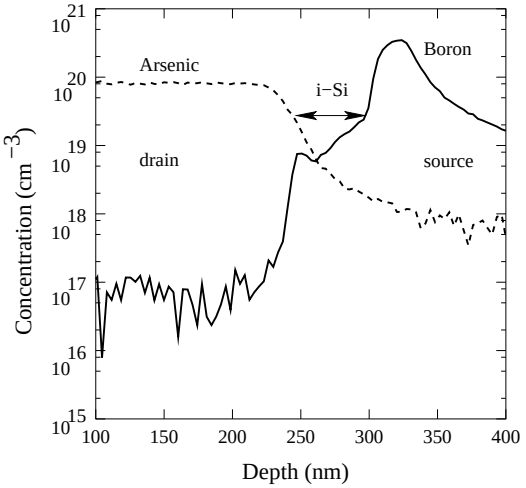

Fig. 2. SIMS doping profile of the tunnel FET.

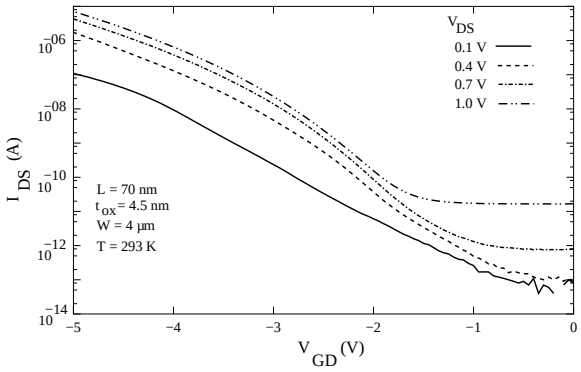

Fig. 3. P-channel transfer characteristics of the 70 nm tunnel FET.

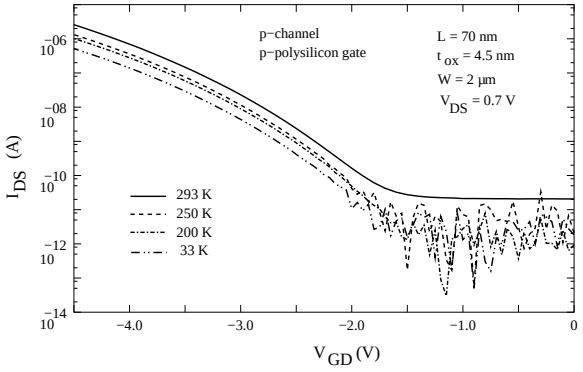

Fig. 4. Low temperature transfer characteristics of the 70 nm tunnel FET at $V_{DS} = 0.7$ V.

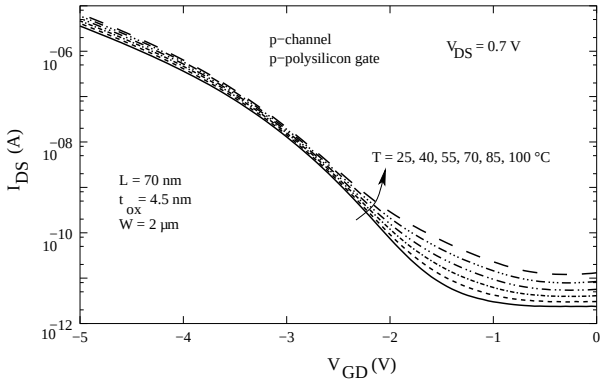

Fig. 5. High temperature transfer characteristics of the 70 nm tunnel FET at $V_{DS} = 0.7$ V.

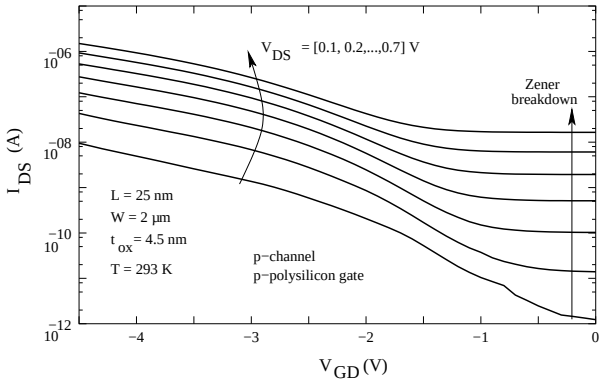

Fig. 6. P-channel transfer characteristics for a 25 nm tunnel FET. Due to smear-out of doping profile, the device breaks down earlier.