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High Mobility Fully-Depleted Germanium-on-Insulator pMOSFET with 32-nm-Thick Ge Channel Layer Formed by Ge-Condensation Technique

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1. Introduction

A Fully-Depleted (FD) Ultra-Thin-Body (UTB) Ge-on-Insulator (GOI) Metal-Oxide-Semiconductor-Field-Effect-Transistor (MOSFET) has attracted much attention as a promising candidate for CMOS device structures in future technology nodes, because of high mobility of germanium channel and steep sub-threshold characteristics. However, FD type GOI-MOSFETs have not been realized yet. For realization of FD-GOI devices, we have fabricated an ultra-thin GOI layer[1] by oxidizing a SiGe layer grown on an SOI layer, which is called the Ge-condensation technique[2]. In this paper, we report, for the first time, the successful fabrication of FD-GOI-pMOSFETs with a 32-nm-thick GOI channel layer and a thermal SiO_2 gate insulator, and demonstrate the device operation with the mobility of 3.1 times larger than the universal one for Si pMOSFETs.

2. Fabrication of GOI-pMOSFET

Fabrication process of a GOI layer by the Ge-condensation technique is summarized in Fig. 1. At first, a SiGe layer of 200 nm with 15 % Ge content was grown epitaxially on a 6-inch (100) silicon-on-insulator (SOI) wafer by the low-pressure chemical vapor deposition (LP-CVD) technique (Fig. 1(a)). The wafer was oxidized in 100 % O_2 at temperatures between melting temperatures of SiGe, which depend on Ge content, and a minimum temperature of 900 °C (Fig. 1(b)). In the oxidation process, Si atoms in the SiGe layer were oxidized selectively and Ge atoms were rejected from the SiO_2 layers, resulting in the increase of Ge fraction in the SiGe layer[2]. When all Si atoms were consumed, we stopped the oxidation and, consequently, obtained a 32-nm-thick-GOI layer (Fig. 1(c)). The formation of a pure GOI layer was examined from the extinction of peaks of Si-related vibration modes in Raman spectra (Fig. 2). Here, the peak position of Ge-Ge mode was identical to that of unstrained bulk Ge, implying that the strain in the GOI layer was completely relaxed. Residual Si content in the GOI layer was also estimated by SIMS technique to be lower than 0.01 %[3]. In addition, Ge oxides (GeO, GeO_2) were not observed (less than the detection limit of 1%) at the SiO_2/GOI interface by electron spectroscopy for chemical analyses (ESCA). From an AFM image of the GOI surface after removing SiO_2 in Fig. 3, a clear crosshatch pattern was observed, suggesting that the relaxation was dislocation mediated[4]. The surface oxide layer of the obtained GOI substrate was utilized as the gate insulator for GOI-pMOSFETs which was thinned to be T_{ox} of 10 ~ 20 nm, by wet etching with diluted HF. The fabrication process of GOI-pMOSFETs is summarized in Fig. 4, in which Si control devices were also processed simultaneously. Figure 5 shows a cross-sectional TEM image of the GOI-pMOSFET with a 32-nm-thick GOI. It is confirmed that the uniform GOI layer and its flat interfaces with gate and buried oxide is formed.

3. Electrical Characterization

Figure 6 shows the gate overdvrive, $V_g - V_{th}$, dependence of drain current, I_d, of GOI device with L/W = 100μm/100μm. Here, since the off-leak current at $V_g = V_{th}$, I_d^0, between source and drain was not negligible as shown in the inset, it was subtracted from I_d. The I_d-V_d characteristics of a Si control device with L = 100 μm are also shown as broken lines for comparison in Fig. 6. It is found that the GOI device exhibited ~3.6 times I_d values of that for the Si control device. The GOI device also showed 2.7 times of maximum tranceconductance than that of the Si control device (Fig. 7), which is corresponding to 3.2 times enhancement for the normalized value by T_{ox}.

The hole mobility of the GOI and the Si control devices was evaluated by split *C-V* measurements. The results are shown in Fig. 8, together with the universal hole mobility in a Si pMOSFET[5]. Hole mobility of the GOI device amounted to 3.1 times of the universal mobility at E_{eff} of ~ 0.2 MV/cm, which is consistent with the drive current and the tranceconductance enhancement in Fig. 6 and Fig. 7, respectively. The mobility enhancement factor is larger than that of a GOI-pMISFET with a high-k gate insulator (× 2.5) [6] and closer to the bulk hole mobility ratio of Ge to Si (~ 4). The high enhancement factor of the present GOI devices fabricated by the Ge-condensation process is attributable to the thermal SiO_2 gate insulator with the smooth interface, presumably due to the oxidation at temperature of as high as 900 °C in the Ge-condensation process. The smooth SiO_2/GOI interface is confirmed in the cross-sectional TEM image in Fig. 9 (a). On the other hand, the plan-view TEM image of a GOI layer (Fig. 9 (b)) shows planer defects (observed as lines) and threading dislocations, which could be the origin of the off-leak current. It is expected, however, that these imperfections along with the

surface roughness did not degrade significantly the hole mobility, considering the large enhancement in mobility.

5. Summary

We reported the successful fabrication of FD-GOI-pMOSFETs using a GOI wafer formed by the Ge-condensation technique, and demonstrated the device operation. It was found that GOI-pMOSFETs with L/W = 100μm/100μm have 3.1 times larger hole mobility than the Si universal hole mobility. Thermal SiO_2 gate insulator formed in the Ge-condensation process is considered to contribute to the high mobility of the GOI device, which may be mainly due to the smooth oxide interface formed by high temperature oxidation.

Acknowledgements

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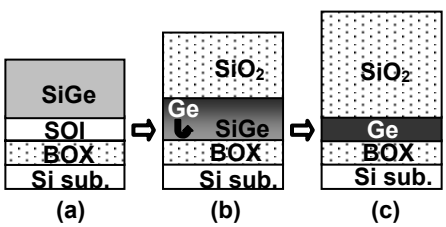

Fig. 1 Fabrication process of GOI layer by Ge-condensation technique.

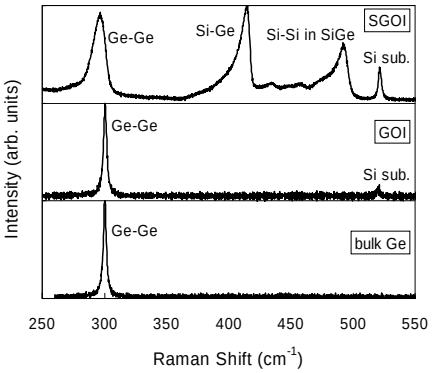

Fig. 2 Raman spectra of SGOI and GOI layers and unstrained bulk Ge.

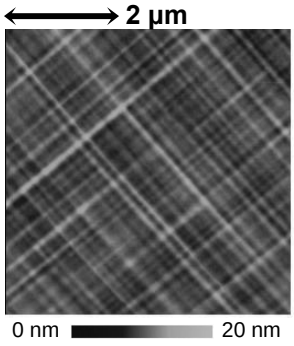

Fig. 3 AFM image of GOI layer. The surface roughness of the GOI layer was estimated to be 1.3 nm (rms) in 10 μm square.

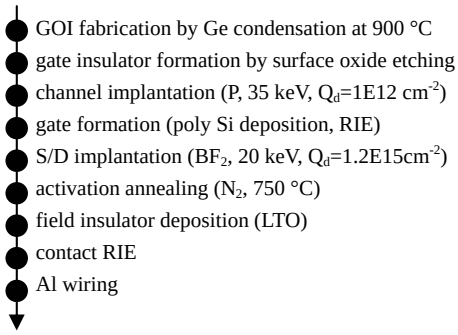

Fig. 4 Process flow for GOI-pMOSFET

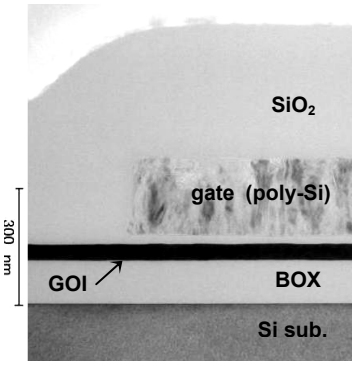

Fig. 5 Cross-sectional TEM image of GOI-pMOSFET.

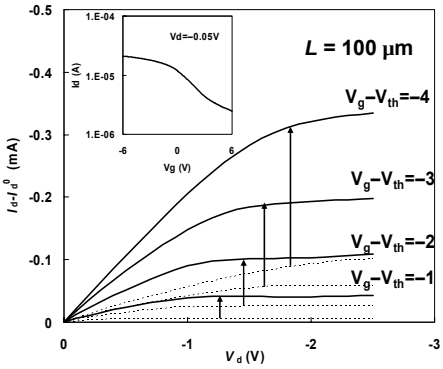

Fig. 6 I_d-V_d characteristics of GOI (solid lines) and Si control (broken lines) devices with L/W=100μm /100μm. Inset shows the I_d-V_g characteristics of GOI device.

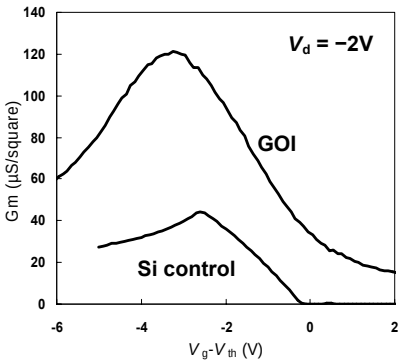

Fig. 7 Tranceconductance of GOI (T_{ox} = 20 nm) and Si control (T_{ox} = 17 nm) devices.

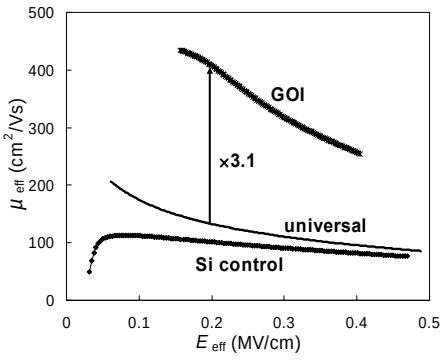

Fig. 8 Effective hole mobility of GOI and Si control devices and universal one in Si pMOSFET.

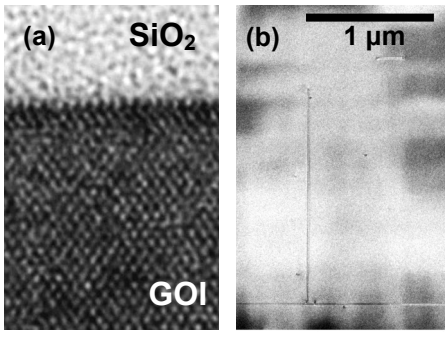

Fig. 9 Cross-sectional (a) and Plan-view (b) TEM images of GOI layers.