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Influence of bulk bias on NBTI of pMOSFETs with ultrathin SiON gate dielectric

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1. Introduction

The negative bias temperature instability (NBTI) of p-MOSFETs has become one of the most crucial reliability issues, especially when the gate oxide thickness is scaled down to less than 2nm and nitrogen is incorporated [1]. Considerable work has been done in both dc and ac NBT stresses, in which a voltage is applied on the gate electrode (V_g) and the source/drain and substrate (bulk, V_b) electrodes are grounded. It was reported that the positive bulk bias during the NBT stress has no influence on NBTI for V_b up to 4V [2,3]. But we find that the degradation can be enhanced significantly by V_b, and the enhancement depends on both V_g and V_b. Moreover, we find, for the first time, that the degradation can be dramatically enhanced under bipolar BT stress if the bulk electrode is floating. Both phenomena suggest that the interface trap generation during the BT stress is closely related to the tunneling of hole from Si to oxide, which can be enhanced by high V_b or the trapped electrons at the interface states during the bipolar BT stress.

2. Devices fabrication and NBTI characterization

The tested p-MOSFETs were fabricated on n-well of p-Si substrates using a standard process with LDD, P^+ poly gate, and plasma-nitrided gate oxide, which has a base oxide thickness of ~ 2nm and a peak nitrogen concentration of 9%. The device was stressed at 125°C, by applying a dc or ac voltage on the gate while source/drain grounded and the bulk electrode is grounded, positive biased or floating. The ac voltage has a square waveform of 50% duty factor and 4.5ns rise and fall time. Immediately after stress interruption, and I_d-V_g and a modified direct-current current-voltage (DCIV) measurement [4] were carried out at the same temperature. Each stress was carried out on a fresh device whose initial interface trap density (N_{it}) is between 1.5~ 3.0×10^9 cm^{-2} for all tested devices.

3. Results and discussion

With increasing the stress time, the DCIV peak increases and the peak positive shifts to the negative direction (Fig. 1), indicating the interface trap generation (ΔN_{it}) and the fixed oxide charge buildup (ΔN_{ot}). Fig. 2 shows the threshold shifts (ΔV_{th}), which are extracted from the I_d-V_g curves, as a function of stress time under various V_g and V_b. Fig. 3 shows the corresponding ΔN_{it} data extracted from the DCIV peaks (e.g. Fig. 1). Both figures show similar trends, i.e., at low $|V_g|$ (1.5V), ΔV_{th} (and ΔN_{it}) is almost independent of V_b (up to 2V), while at $|V_g| \geq 2.0$V, it is significantly enhanced by V_b = 2V. The enhancement magnitude depends on both V_g and V_b. The higher $|V_g|$, the lower V_b to trigger the enhancement is. It should be noted that our finding is different to those reported by Y. Mitani *et al.* [3] and V. Huard *et al.* [2], where $|V_g-V_{th}|$, rather than V_g, kept the same. For simplification, only ΔN_{it} data are shown following.

Under ac NBT stress (both unipolar and bipolar), similar V_b effect still exists (Fig. 4), while the enhancement magnitude is decreased under the bipolar stress. On the other hand, with the bulk electrode floating, ΔN_{it} is dramatically enhanced under the bipolar stress while it remains almost unchanged under the dc or unipolar stress (Fig. 5). ΔN_{ot} is enhanced more significantly than ΔN_{it} (not shown here).

In normal bipolar BT stress (V_b=0), the ΔN_{it} enhancement occurs at frequency larger than ~ 10 kHz [5]. With V_b floating, the enhancement magnitude is much larger and the enhancement occurs at 1 Hz and then saturates or increases very slowly at frequency larger than 1 kHz (Fig. 6). At the early stress time, ΔN_{it} increases with time in a power-law but with the exponent n much larger than 0.25 (Fig. 7), indicating that there is an additional mechanism for both ΔN_{it} and ΔN_{ot}. The decrease of the increase rate at the longer stress time can be ascribed to the passivation effect [5]. The effects of the stress voltage magnitude are shown in Figs. 8 and 9. The enhancement occurs when the positive voltage (V_+) of the unsymmetrical bipolar waveform is larger than about 1.3V.

It is well known that ΔN_{it} (also ΔN_{ot}) is closely related to the holes in the inversion layer. We speculate that it is not the total density of holes, but the density of high-energy holes that can tunnel into oxide, plays a role to the ΔN_{it} (and ΔN_{ot}). In the $V_b = 0$ case, the holes are the "cold" holes, and are excited only by temperature. If $V_b > 0$, the holes can be accelerated by the bulk voltage, therefore the tunneling probability is significantly enhanced even though the total hole density is reduced due to the reduction of $|V_g-V_{th}|$ [6]. In the case of bipolar stress with V_b floating, the electrons trapped at the interface or near-interface states can not follow the applied V_g variation. The build-in electric field originated from the trapped electrons can accelerate the hole tunneling when V_g shifts from positive to negative, thus enhance the ΔN_{it} generation. Because the electrons are trapped at the upper half of the band gap, the V_+ to trigger this enhancement should be larger than the middle-gap voltage (V_{mg}), as confirmed by Fig. 9.

Our finding indicates that, in some cases that the bulk electrode is floating, e.g. for SOI devices without body contact, a dramatic degradation may occur under bipolar stress. On the other hand, very large V_{th} shift (e.g., >1V) can be obtained at a relatively small $|V_g|$ by floating V_b and applying a bipolar V_g.

4. Conclusion

The V_b (grounded, positive biased, or floating) effects on both dc and ac NBTI are studied. The positive bulk bias can enhance the ΔN_{it} generation significantly under dc and unipolar ac stresses. Moreover, a dramatic ΔN_{it} enhancement is observed under the bipolar BT stress with V_b floating. We suspect that the enhancement is due to the

enhanced tunneling probability, originated from the positive V_b or the trapped electrons in the bipolar stress case.

Acknowledgements

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References

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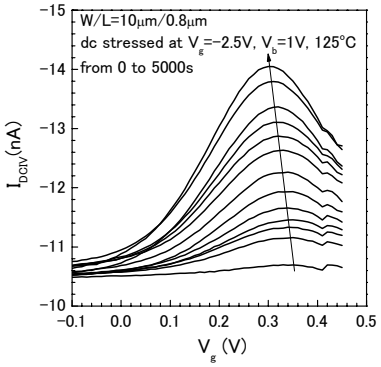

Fig. 1 DCIV curves using a modified DCIV method [4] as a function of stress time. The DCIV peak is proportional to N_{it}, while the peak position shift is related to ΔN_{ot}.

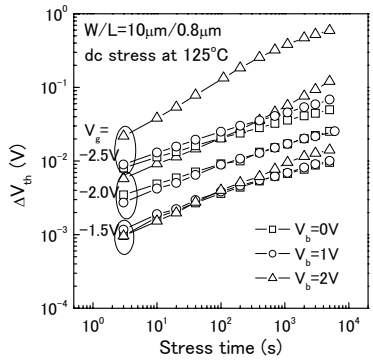

Fig. 2 The threshold voltage shift, which is extracted from the I_d-V_g curves, as a function of stress time under dc stress with various V_g and V_b. The ΔV_{th} is significantly enhanced at V_b = 2V.

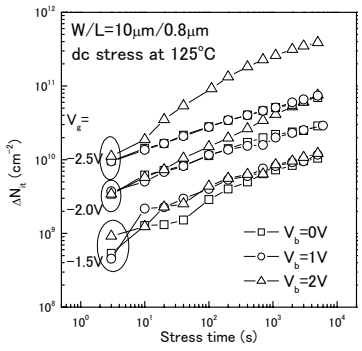

Fig. 3 The interface trap generation, which is deduced from the modified DCIV curves, as a function of stress time under dc stress with various V_g and V_b, it has the similar trend as ΔV_{th}.

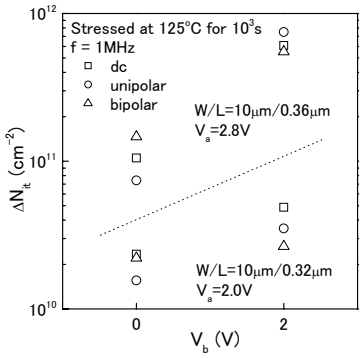

Fig. 4 The interface trap generation under dc, uniolar or bipolar pulsed stresses at V_b = 0 or 2V. Compare to the dc case, unipolar stress has similar V_b effect, while the enhancement is smaller at the bipolar case.

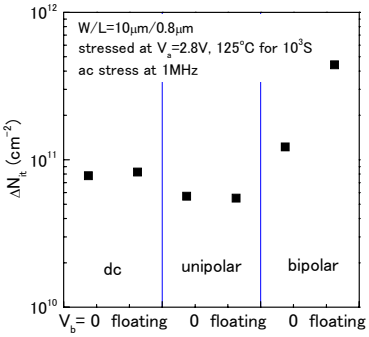

Fig. 5 The interface trap generation under dc, unipoar or bipolar at V_b grounded or floating. ΔN_{it} is dramatically enhanced under bipolar stress if V_b is floating.

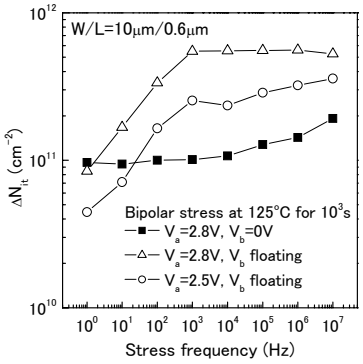

Fig. 6 The stress frequency dependence of the interface trap generation under bipolar BT stress with V_b floating or grounded. With V_b floating, ΔN_{it} increases remarkably with frequency and then saturates at frequency larger than ~ 1kHz.

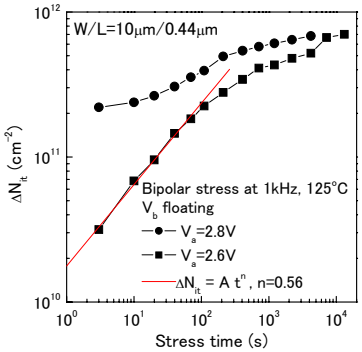

Fig. 7 The time evolution of the interface trap generation under bipolar stress with V_b floating. The reduction of the increase rate at the larger ΔN_{it} region is probably due to the passivation effect.

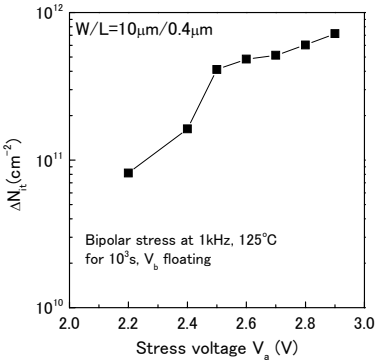

Fig. 8 The interface trap generation under bipolar stresses with V_b floating as a function of the stress voltage magnitude (V_a). The ΔN_{it} increase rate slows down when V_a is larger than ~ 2.5V.

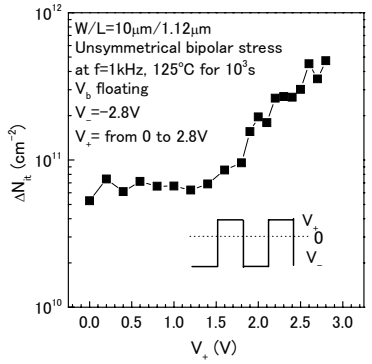

Fig. 9 ΔN_{it} as a function of V_+ under unsymmetrical bipolar stresses with V_b floating. Inset shows the schematic waveform. The enhancement occurs when V_+ is larger than ~ 1.3V.