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# Devices Characteristics and Aggravated Negative Bias Temperature Instability in PMOSFETs with Uniaxial Compressive Strain

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## 1. Introduction

Down scaling of metal-oxide-semiconductor field-effect transistors (MOSFETs) suffers from carrier mobility degradation due to increased channel doping necessary for suppressing the short-channel effects. Recently, mobility enhancement by introducing channel strain has emerged as an effective approach to alleviate the restriction [1-7]. This could be done by either applying high biaxial tensile strain to the channel region with a SiGe virtual substrate [1-2], or by uniaxially straining the channel with strain boosters [3-7]. The approach of using SiGe virtual substrate, however, suffers from a number of drawbacks such as Ge up-diffusion and high defect density. In contrast, the approach of uniaxially straining the channel is essentially free of the aforementioned drawbacks. It is thus more suitable for practical manufacturing. However, the reliability issue of the devices would be a potential concern when the local strain is introduced, and should therefore be carefully addressed. In this work, we investigate the negative bias temperature instability (NBTI) of PMOSFETs with compressively strained channel.

## 2. Device Fabrication

The PMOSFETs used in this study were with 3 nm thermal oxide as the gate dielectric, and 150 nm poly-SiGe layer as gate material. SiN capping and TEOS passivation layers were deposited by PECVD. The precursors for SiN deposition were $SiH_4$ and $NH_3$. The SiN capping had been shown previously to introduce significant compressive strain to the channel of PMOSFETs [3,4]. Contact holes and metallization processes were subsequently performed. Finally, the processing steps were completed with a forming gas anneal at 400 ˚C. Electrical characterizations were performed using an HP4156 system. NBTI stress measurements were performed at 125 ˚C. The interface traps were evaluated using the charge pumping method with a fixed amplitude of 1.5 V at 1 MHz.

## 3. Results and Discussion

The stress from PE-SiN layer was first examined by probing blanket monitor samples deposited on Si wafers. We confirmed that the stress is compressive and increases monotonically with increasing thickness. The stress is around –95 MPa for 100 nm SiN. Fig. 1 compares output characteristics of PMOSFETs with and without SiN capping layer. It can be seen that the drive current is increased when the SiN capping layer is incorporated. The transconductance values of the devices exhibit similar improvement, as shown in Fig. 2. These observations are consistent with the film stress measurements, and also with the results reported previously with compressive SiN capping [3,4].

Figure 3 shows the percentage increase of the drive current of the SiN-capping device, compared to the control devices, as a function of channel length. When the channel length is less than 1 μm, the drive current increases sharply because of enhanced effect of local strain in shorter channel devices. Nevertheless, the subthreshold characteristics of the devices do not seem to be affected by the induced strain, as shown in Fig. 4. When operating at a raised temperature (e.g., 125 $^{o}$C), the device characteristics illustrated in Figs. 5 and 6 show basically the same trends as those observed at room temperature.

Figs. 7 and 8 show the results of NBTI stress performed at three different gate biases. As can be seen in the figures, larger changes in threshold voltage shift, $\Delta V_{th}$, are observed in the device with SiN capping. The shift curves show a fractional power-law dependence on time ($\Delta V_{th} \propto t^{n}$), and the values of the exponent are roughly 0.2 and 0.3 for samples without and with SiN-capping layer, respectively.

Increase in interface state density, $\Delta N_{it}$, is also larger for the SiN-capping samples, especially at high temperature (Fig. 9). It is noted that $\Delta V_{th}$ and $\Delta N_{it}$ approach saturation for the device with SiN capping when NBTI stress time exceeds 1000 sec. From Fig. 10, the maximum value of transconductance, $GM_{max}$, degrades gravely in the device with SiN layer. The above results clearly indicate that the use of PECVD SiN capping may result in aggravated NBTI. It may be due to higher density of Si-H bonds at the oxide/Si interface. The extra hydrogen species are from the SiN layer as a result of using $SiH_4$ and $NH_3$ as precursors. Higher strain energy stored in the channel may also play a role in the aggravated degradation process: the energy may help trigger the electrochemical reactions at the interface. This is consistent with the higher exponent value of the power-time dependence for devices with SiN capping.

## 4. Conclusion

Compressive PECVD SiN layer could significantly enhance the drive current of PMOS devices at room and raised operating temperatures (125 $^{o}$C). Despite this coveted merit, our results indicate that the SiN capping may aggravate the NBTI characteristics. A high amount of hydrogen species contained in the PE-SiN layer as well as the strain energy stored in the channel may be the culprits for the worsened reliability.

**Acknowledgments**

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**Reference**

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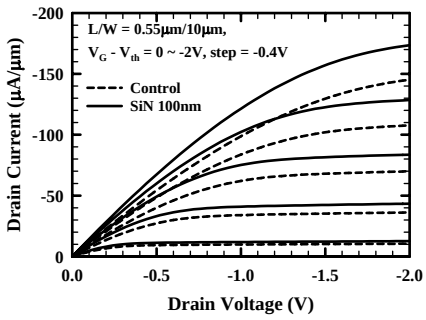


Fig. 1 Output characteristics of PMOSFETs with and without PE-SiN layer.

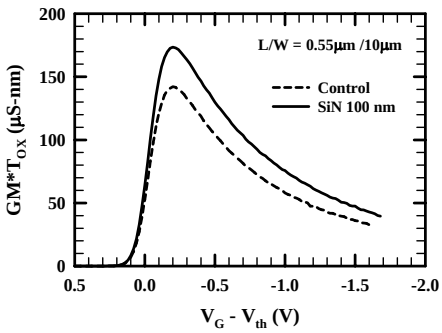


Fig. 2 Transconductance × $T_{OX}$ versus $V_G$ – $V_{th}$ for PMOSFETs with and without PE-SiN layer.

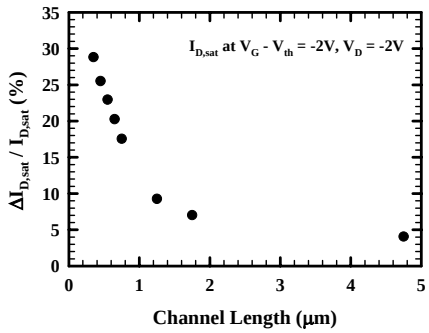


Fig. 3 Drain current increase percentage of PMOSFETs with and without PE-SiN layer. Drain current measured at $V_G$-$V_{th}$ = -2V and $V_D$ = -2V.

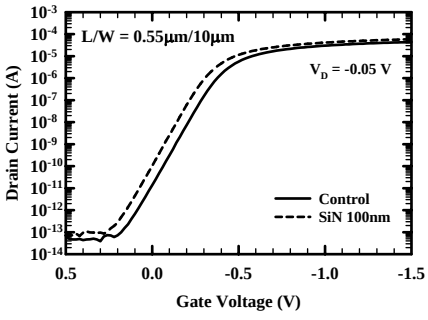


Fig. 4 Subthreshold characteristics of PMOSFETs with and without PE-SiN layer.

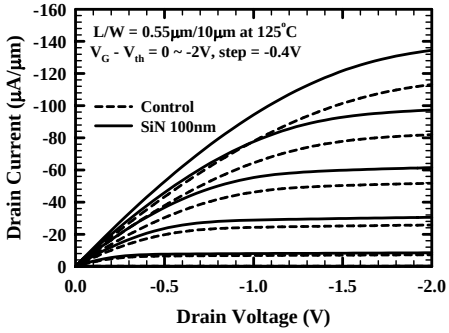


Fig. 5 Output characteristics of PMOSFETs with and without PE-SiN layer at 125 °C.

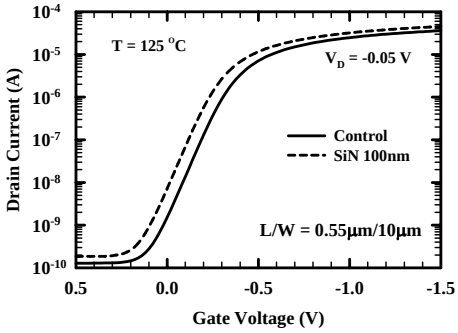


Fig. 6 Subthreshold characteristics of PMOSFETs with and without PE-SiN layer at 125 °C.

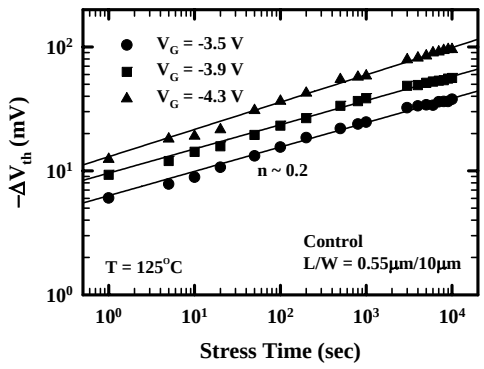


Fig. 7 $\Delta V_{th}$ versus stress time at three different gate biases for control sample.

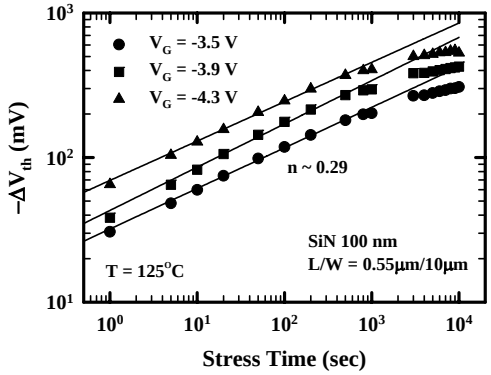


Fig. 8 $\Delta V_{th}$ versus stress time at three different gate biases for SiN 100nm sample.

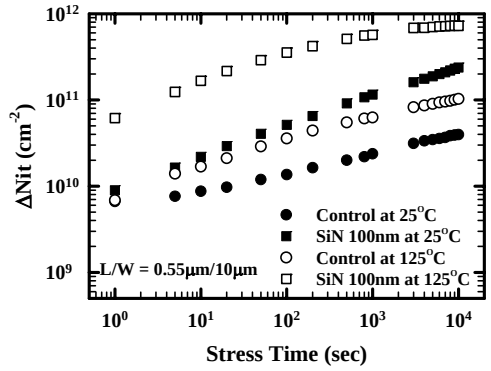


Fig. 9 $\Delta N_{it}$ versus stress time at 25 °C and 125 °C. $\Delta N_{it}$ of PMOSFET with PE-SiN layer increases greatly and nearly saturates at 125 °C.

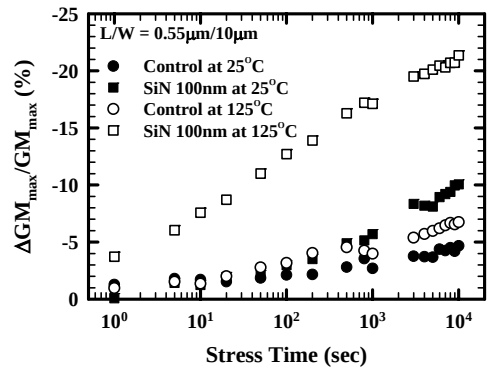


Fig. 10 Transconductance degradation versus stress time at 25 °C and 125 °C. Transconductance of PMOSFET with PE-SiN layer degrades gravely at 125 °C.