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Efficient Reduction of Standby Leakage Current in LSIs for Use in Mobile Devices

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Introduction

Transistors for mobile devices require higher performance and lower power consumption. At the same time, we are required to decrease the standby leakage current (Isb). Many studies have reported on methods of forming low-leakage transistors. However, off-state current (Ioff) must be further reduced. 65-nm node or less is not suitable for use in LSIs aimed at mobile devices because their gate leakage constitutes the major part of their Ioff, referring to ITRS 2004 update. We believe that a 90-nm node or more would be suitable. With these nodes, the gate-induced drain leakage (GIDL) and sub-threshold leakage current (IS) are dominant. It should be noted, however, that the Ioff is in a "tradeoff" relationship with on-state current (Ion). Our goal is to establish a technology to reduce Ioff down to 0.1pA while keeping Ion at a high level. To achieve that, it is a key to shape the impurity profile which is very different from conventional one. In this report, we propose a new impurity implant method and discuss the electric characteristics of the transistors and an SRAM which accounts for 70% or more of total Isb in LSI.

Impurity Implant Methods for Ioff Reduction

-Shallow Channel-

In an NMOS, IS arises near the channel/shallow trench isolation (STI) interface (Fig. 1). B density decreases near the channel surface that borders with the STI. This phenomenon causes IS to increase sharply. To control the decrease in B density, we distribute B in a very shallow channel region. Fig. 2 shows a center B-depth profile for a channel region. The Rp of the shallow channel we propose is 1.5E-2 um or below, which is far shallower than the B-depth distribution of any conventional method. The desirable ion to be injected is BF_2, which is not so prone to channeling. Moreover, BF_2 is effective for limiting thermally enhanced diffusion. Conventional methods use an impurity profile called retrograde or super-steep retrograde (SSR), which improves a carrier mobility at the 65-nm node [3]. However, to keep B density under control, the shallow channel is more effective as shown in the following.

-Asymmetric Implant-

Until now, a pocket implant in four directions is made on the source and drain sides. To decrease IS even more we only make a tilted pocket implant on the source side which casts a shadow of gate electrode on the drain side (Fig. 3). Asymmetric implant has been used to improve carrier mobility [4]. In our proposal, we improve carrier mobility and raise the threshold voltage (Vth) without lowering Ion, which effectively reduces IS. For Ioff in a PMOS, the substrate leakage current (IB) is dominant due to GIDL which arises at the edge of gate electrode on the drain side. Asymmetric implant from the source side is effective in decreasing IB. To make the SRAM layout compatible with asymmetric implant, we used the transistor layout shown in Fig. 4. The sources and drains for the driver and load transistors all face the same direction. To hinder transistor density as little as possible, we only increased cell dimension 17% or less in relation to a conventional layout.

Electric Characteristics of a Low Leakage Transistor

Fig. 5 shows the relation between Ioff and Ion for an NMOS using shallow channel and asymmetric implant. The control is made by SSR and symmetric pocket implant. The gate length and width (W) are 0.18 and 1 um and the drain voltage is 1.8 V. Both methods successfully decrease Ioff by 80% or more while maintaining Ion at a high level. Ioff is 0.1pA. Fig. 5 also plots Ion-Ioff results from other reports [1, 2]. In the previous studies, Ion was in a "tradeoff" relationship with Ioff. This meant that transistor performance would become significantly worse as Ion decreased. Fig. 6 shows IS in relation to W. The level of IS in the control remains high throughout the zone in which W varies. This result proves that the leakage component in the interface between the channel and the STI is dominant. IS for the shallow channel decreases with W before reaching 0.3 um, the point at which the inverse narrow channel effect starts to appear. This result proves that the decrease in the density of B is controlled well. The plot for shallow channel followed by asymmetric implant shows even more IS reduction. Fig. 7 shows the relation between Ion and Vth for an NMOS with asymmetric implant. Where Ion is the same for the Control and the asymmetric implant plot, the Vth of the latter is higher. When the dose of the asymmetric implant is doubled, Vth becomes even higher. This result shows improvement in the carrier mobility of the asymmetric implant. Asymmetric implant is thus effective in IS reduction.

For a PMOS with asymmetric implant, Ioff can be decreased to 0.1pA while maintaining a high level of Ion (Fig. 8). Fig. 9 shows IB in relation to changes in W. The asymmetric implant plot shows a significant reduction in IB.

SRAM Standby Leakage Characteristics

Fig. 10 shows the schmoo plots for a 1.3-Mb SRAM. The SRAM that uses the above methods shows the same speed performance as the Control. Fig. 11 shows Ioff for each SRAM transistor. The shallow channel can effectively reduce IS for a driver and a transfer transistor. Shallow channel followed by asymmetric implant is even more effective for a driver transistor, reducing Ioff by 61% compared to the shallow channel. Asymmetric implant is also effective on a load transistor, effectively reducing the IB and reducing Ioff by 81%. Fig. 12 shows Isb for a 1.3-Mb SRAM. Compared to the Control, the Isb of shallow channel is reduced by 50%. For shallow channel followed by asymmetric implant, the Isb is reduced to one-tenth.

Conclusion

Shallow channel and asymmetric implant methods can maintain Ion at a high level and, at the same time, reduce Ioff down to 0.1pA. The impurity profile we propose is very different from conventional one. We have successfully reduced Isb in large-scale SRAM by a significant amount and maintained high-speed performance. We are confident that our new method will make a significant contribution toward Ioff reduction in mobile devices.

References

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[2] C. C. Wu et al., IEDM Tech. Dig., pp.671-674, 1999.
[3] S. Zhao et al., Symp. on VLSI Tech., pp.14-15, 2004.
[4] Baohong Cheng et al., IEEE Electron Device Lett., vol. 20, No. 10, Oct. pp.538-540, 1999.

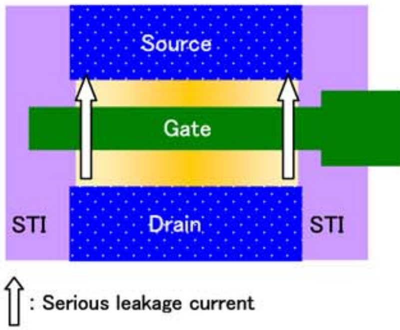

Fig. 1. Serious IS leakage current occurs at the channel/STI interface.

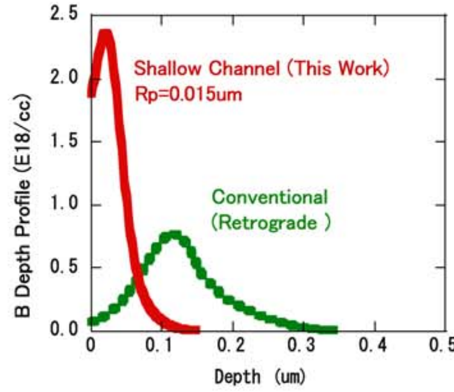

Fig. 2. B-depth profiles at the channel center for shallow and conventional channels.

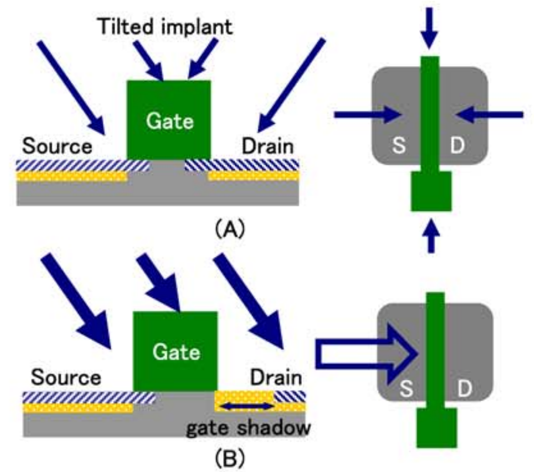

Fig. 3. Comparison between conventional implant (A) and asymmetric pocket implant (B) .

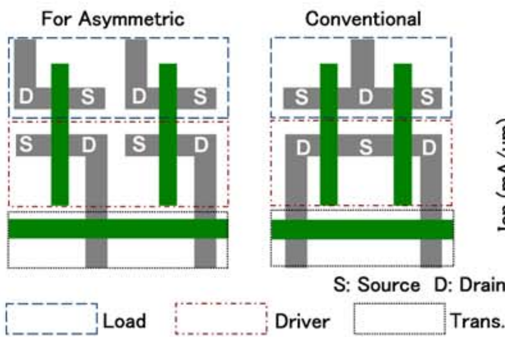

Fig. 4. Proposed SRAM cell layout for asymmetric implant.

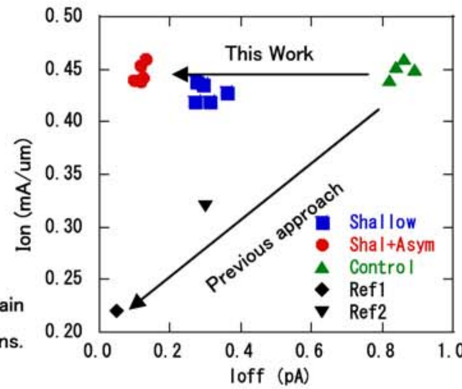

Fig. 5. Ion and Ioff are compared using NMOS low-leakage transistors along with previous data (Ref. 1, 2).

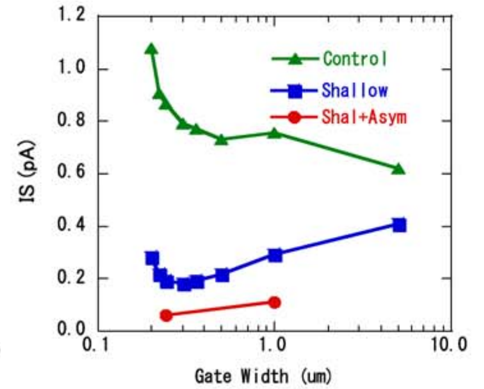

Fig. 6. Relation between IS and gate width for an NMOS low-leakage transistor.

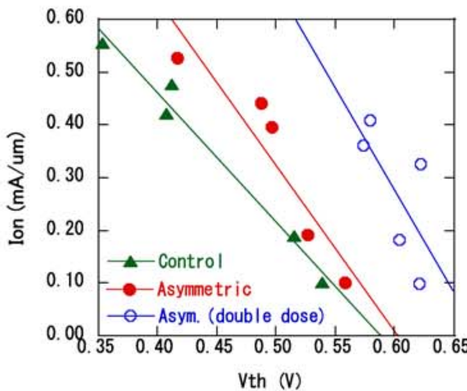

Fig. 7. Relation between Ion and Vth for an NMOS transistor with asymmetric implant.

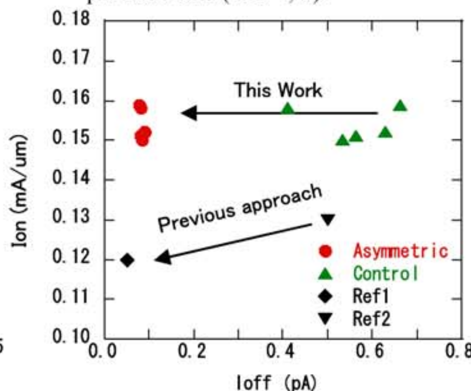

Fig. 8. Ion and Ioff are compared using PMOS low-leakage transistors along with previous data (Ref. 1, 2).

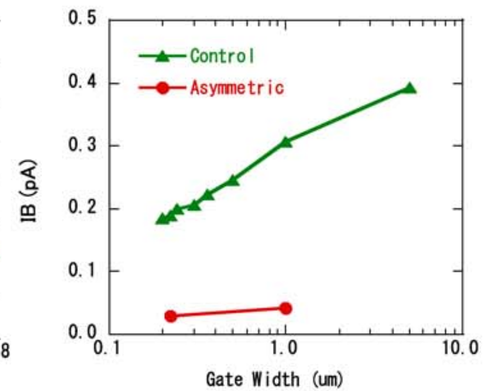

Fig. 9. Relation between IB and gate width for a PMOS low-leakage transistor.

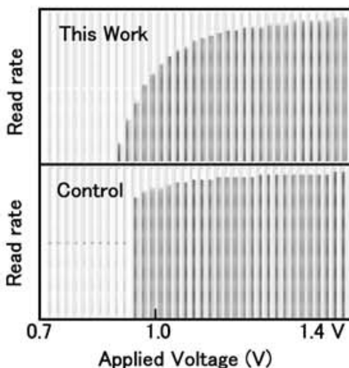

Fig. 10. schmoo plots for a 1.3-Mb SRAM.

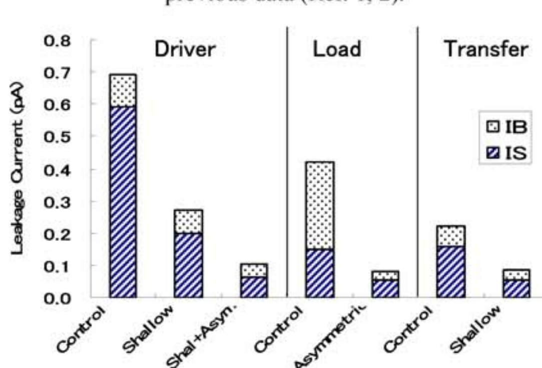

Fig. 11. Leakage components of various types of SRAM transistors.

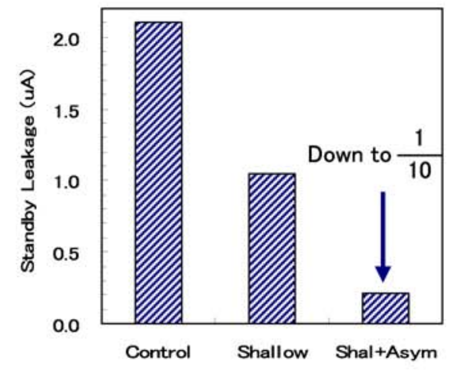

Fig. 12. Standby leakage current of 1.3-Mb SRAM.